

Model Name: GA-H87-D3HP

1.0

SHEET

TITLE

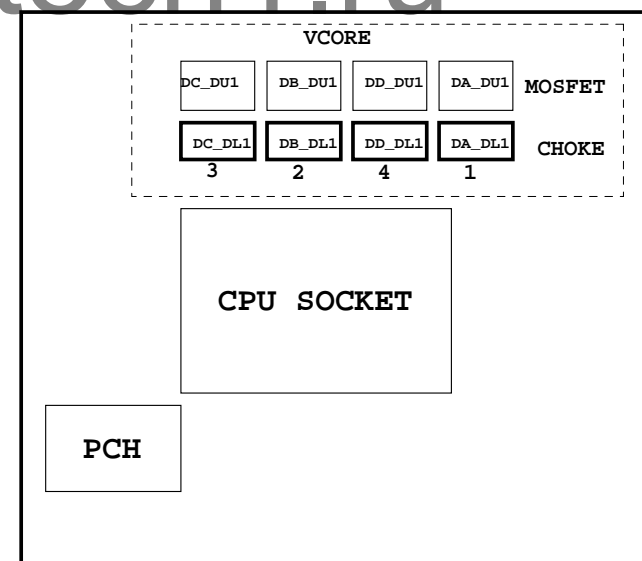
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B
06	CPU_LGA1150-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE
10	PCH_RGB,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCIEX1*2 , PCIEX4 SLOT
16	ITE8892 PCI BRIDGE
17	PCI SLOT 1&2
18	I/O ITE8728
19	COM, -PROHOT, R_USB
20	Dual BIOS , TPM SLB9635TT
21	ALC892 CODEC
22	REAR AUDIO JACK
23	VCORE PWM_IR3564a
24	VCORE+DDR PWM IR3553+IR3598
25	ME POWER
26	NCP3933 OVER VOLTAGE
27	DISCRETE POWER

SHEET

TITLE

28	F_PANEL , F_USB2.0/3.0
29	ATX POWER, CLOCK GEN
30	HWM , KB/MS , FAN CTRL
31	LAN INTEL i217
32	DVI
33	HDMI , R_USB30
34	TABLE LIST
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Title			
Cover Sheet			
Size	Document Number	GA-H87-D3HP	Rev
Custom			1.0
Date:	Monday, April 01, 2013	Sheet	1 of 38

## GA-H87-D3HP

## Component value change history

Data	Change Item	Reason
0.1-0925	E-BOM	
	1. Z77-D3H改為削光黑PCB, slots同原本削光黑機種配色, CPU socket線黑	
	2. 8 series IR digital power PWM因Intel spec change, 須改用b版 (必須發行Firmware)	
	3. H77-D3H 注意上H87 chips, 上ME power, 咖啡黑機種配色, CPU socket standard, clock buffer要上	
	3. H77-D3H GPIO37 需Pull up to 3VDUAL	
0.2	1. Load-line DAR47 2.06K --> 2.37K , DAR46/50 1.4K --> 1.6K , DAC17 150P --> 100P	
	2. N_-LAN_WAKE NR60 8.2K/4 --> 1K/4/1	
	3. DA_DUI, DB_DUI, DD_DUI, DC_DUI 10IFB-403553-01R --> 0TA1-603551-00R	
	4. DDR CHOKER阻值調整	
	5. CPU SOCKET + RM 要用新料號?	
0.2B	1. 確定Power stage用料: IR3553 or IR3550 or 3551?	
	2. GPIO8 "NR136"不上	
	3. Add +12V排阻 RN2-RN6	
0.2C	1. HU1 , HU2 level shifter change to NXP	
0.3	1. PWM MOSFET修改 IR3564B + power stage 改成 IR3564B + IR3535 + power pak (Cancel)	
	3. PWM MOSFET修改 IR3564B + power stage 改成 IR3564B + IR3535 + power pak	
1.0	1. PCIE X16 patch reset circuit 怎麼上?	
	2. Prochot是否只上一組	
	3. PCH_HS & MOS_HS change new 料號	
	4. 因DII 2222禁用, 注意Z87-D3H試產時用Panjit 2222是否可用(BOM已內建)	
	5. HDMI/DVI change to NXP level shifter	
	6. CHECK 5VSB保護線路是否上件	
Z87-D3HP		
1.0A	1. 5VDUAL OVP --> 5VSB OVP	
	2. Remove 全成信PCB	
1.0B	1. Remove DAJP1	
	2. HR29 3.09K --> 3.3K	
	3. USB3.0 HUB add RT9018	

## Circuit or PCB layout change

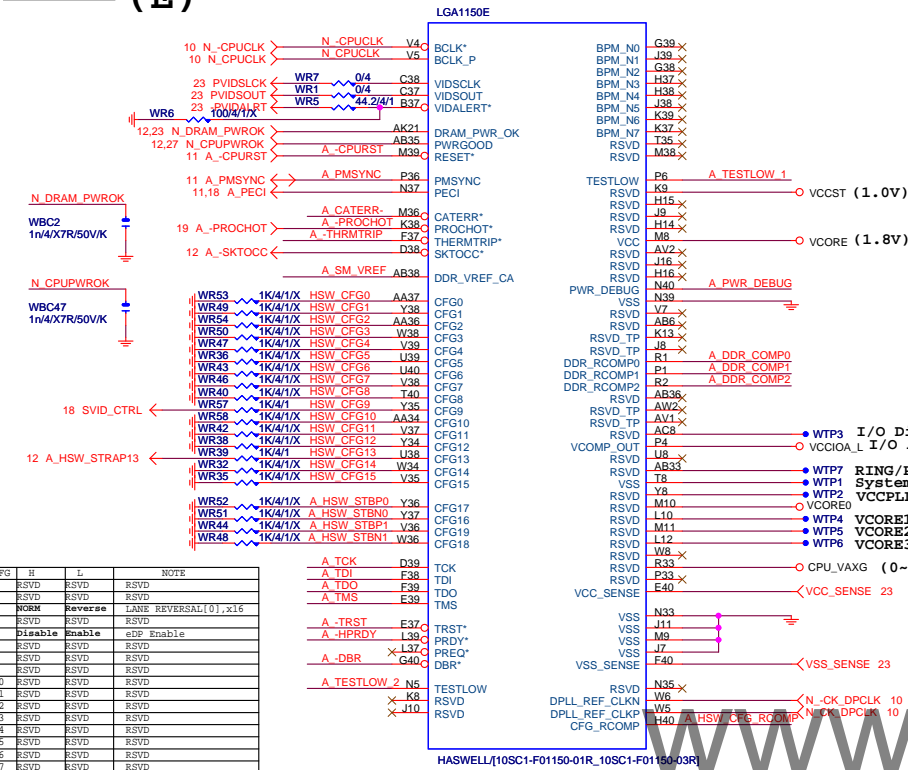
DATE	Change Item	Reason
0.1	E-BOM	
0.2	1. U8 pin3加粗40mils 2. Update LAYOUT NEW RULE for四層板 3. MDA6線長T型要繞等長 4. N_GPIO37 pull up VCC3 --> 3VDUAL 5. CPU Thertrip CPU_VTT --> VCC1_05_PCH 6. 確認 R/G/B ESD擺放位置 7. Add PCIE X16 reset patch circuit 8. PCIE signal by group 成對走 9. VIN0 --> VCORE0 , VIN5 --> VCORE 10. CS 1pin --> 2pin 11. 後窗部份鋪銅會挖 + 字處理 12. Add MA_DR8 , MA_DC8單獨下地 13. add VTT_PWRGD control circit 14. Update F_PANEL footprint "H2X10PANEL-3" 15. NR132跟NC59 layout位置交換 16. Add DS_ME GP67 control 17. Q6位置靠近 PWM power control pin 18. WR59 change to "R0204-2" 19. 文字面 "DualBIOS" , 改為" Dual UEFI BIOS" , Add "Intel GbE LAN" 20. MAU2 REF "GND" 21. DDR Choke ML1, ML2 1.2uH/20A --> 0.8uH/35A	
0.21	1. AUDIO SPDIF-IN CR77 "0402-2" FOR short protection 2. add AUDIO ON/OFF PLAYER 3. Change PCIE X1/PCIE X4 CLK 4. Update F_PANEL footprint 5. CPU VRIN OV IO_GP81 --> IO_GP21	
0.3	1. PWM MOSFET修改 IR3564B + power stage 改成 IR3564B + IR3535 + power pak (Cancel)	
1.0	1. 0 ohm --> short pad 2. 簡化CPU Config setting 3. Remove "BIOS_PH" & "M_BIOS socket" & "CS" pin 4. 注意Slot和後窗正面有做十字Thermal處理 5. NBC65移靠近PCH 6. Add R700-R702 for FAN short protection 7. PWR_LED 改為IO_GP65 8. VTT_PWRGD Update 9. N_GPIO37 pull-up to VCC3 10. +12V RN2-RN6 & VCC/VCC3/5VSB dummy load 排阻 11. DDR_15V H/W monitor detect 改從 DDR slot 拉回 12. 5VSB AD1要過 NET 13. DDR VIN 間隔拉開 , 背板GATE往上移 14. Add DDR_15V dummy load 15. 5VSB/5VDUAL OVP protection 16. 預留N_PCH_DPWROK 控制線路	
Z87-D3HP-0.1	1. add USB3.0 Hub	

Z87-D3HP-1.0 1. DART2改成R0402-2(靠近DD\_DUI) , DART4改成R0603-RH(放在DART2左邊) , RS1改成R0402-2  
2. Add DAR82 For MOSFET "PHSFLT-" protect

Gigabyte Technology			
BOM & PCB MODIFY HISTORY			
Title	Document Number		
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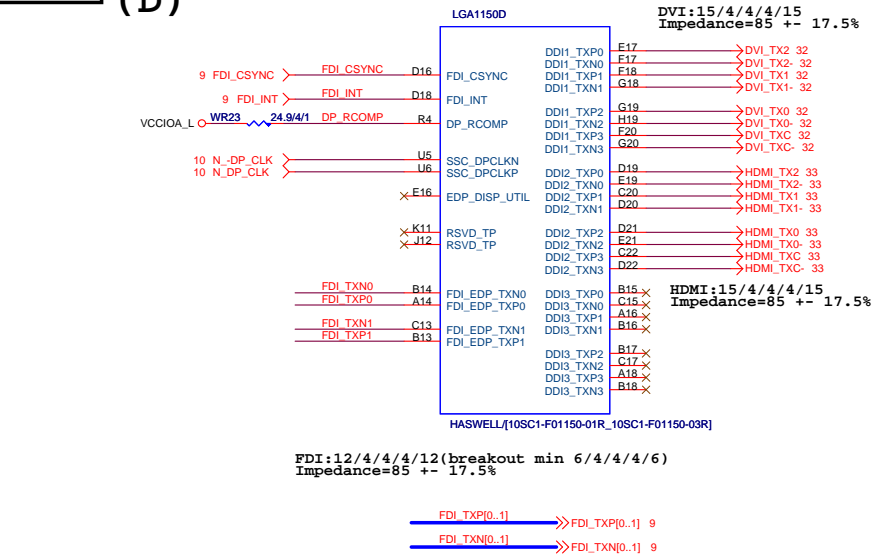
LGA1150 (E)



CFG6	CFG5	PCIE CONFIG
1	1	1x16 , Default
1	0	2x8
0	1	RSVD
0	0	X8, X4, X4

G 0-17 all internal PULL-UP

**LGA1150 (D)**

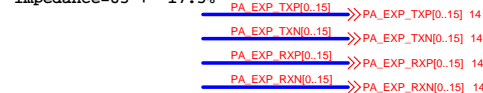


LGA1155 (C)

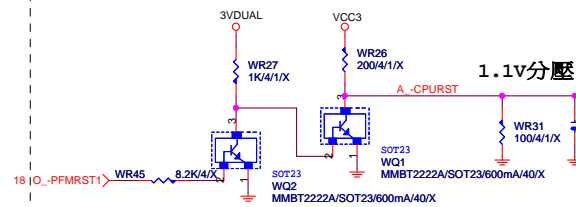
PCIEX16:20/5/4/5/20(breakout min 10/4/4/4/10)  
Impedance=80 +- 17.5%



DMI:12/4/4/4/12(breakout min 8/4/4/4/8)  
Impedance=85 +- 17.5%



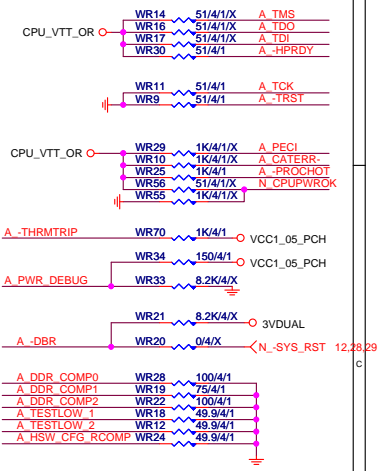
## -CPURST



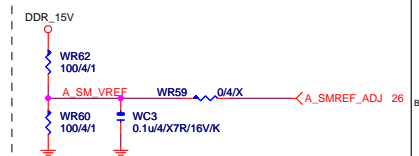
## CPU SVID



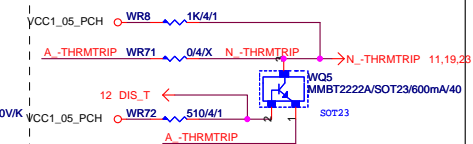
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100	1	1



SM REF
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THRMTRIP DISABLE



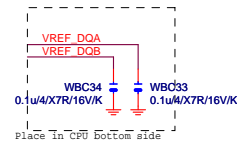
## LGA1150 (A)

LGA1150A	
MAAA0 AU13	DDR0_MA0
MAAA1 AV16	DDR0_MA1
MAAA2 AU16	DDR0_MA2
MAAA3 AW17	DDR0_MA3
MAAA4 AU17	DDR0_MA4
MAAA5 AW18	DDR0_MA5
MAAA6 AV17	DDR0_MA6
MAAA7 AT18	DDR0_MA7
MAAA8 AU18	DDR0_MA8
MAAA9 AT19	DDR0_MA9
MAAA10 AW11	DDR0_MA10
MAAA11 AV19	DDR0_MA11
MAAA12 AU19	DDR0_MA12
MAAA13 AT20	DDR0_MA13
MAAA14 AU20	DDR0_MA14
MAAA15 AU21	DDR0_MA15
MODT_A0 AW10	DDR0_ODT0
MODT_A1 AV2	DDR0_ODT1
MODT_A2 AV9	DDR0_ODT2
MODT_A3 AU8	DDR0_ODT3
AW33	DDR0_ECC0
AW33	DDR0_ECC1
AU31	DDR0_ECC2
AW31	DDR0_ECC3
AU33	DDR0_ECC4
AW33	DDR0_ECC5
AT31	DDR0_ECC6
AW31	DDR0_ECC7
SBA00 SBA01 AV12	DDR0_BA0
SBA00 SBA01 AV11	DDR0_BA1
SBA02 SBA02 AT21	DDR0_BA2
CKEA0 CKEA1 AV22	DDR0_CKE0
CKEA1 CKEA2 AT23	DDR0_CKE1
CKEA2 CKEA3 AU23	DDR0_CKE2
CSEA0 CSA0 AU14	DDR0_CS_N0
CSEA1 CSA1 AV9	DDR0_CS_N1
CSEA2 CSA2 AU10	DDR0_CS_N2
CSEA3 CSA3 AV8	DDR0_CS_N3
DCLKA0 DCLKA0 AY15	DDR0_CLK_P0
DCLKA0 DCLKA1 AY16	DDR0_CLK_N0
DCLKA1 DCLKA1 AW15	DDR0_CLK_P1
DCLKA1 DCLKA1 AV15	DDR0_CLK_N1
DCLKA2 DCLKA2 AW14	DDR0_CLK_P2
DCLKA2 DCLKA3 AW14	DDR0_CLK_N2
DCLKA3 DCLKA3 AW13	DDR0_CLK_P3
DCLKA3 DCLKA3 AY13	DDR0_CLK_N3
AW12	RSVD
RSVD	
-SRASA -SRASA AU12C	DDR0_RAS*
-SWEA -SWEA AU11C	DDR0_WE*
AV20C	RSVD
AV27C	RSVD
-SCASA -SCASA AU9C	DDR0_CAS*
WR61 D4/SH1MX AK22C	DDR_RESET
7.8 -DDR3_RST WC4 0.1u/4X7R/16V/KX	
AD38 MDA0	
AD39 MDA1	
AF38 MDA2	
AF39 MDA3	
AD37 MDA4	
AD40 MDA5	
AE37 MDA6	
AF40 MDA7	
AH40 MDA9	
AH39 MDA13	
AK38 MDA10	
AK39 MDA11	
AH37 MDA12	
AH38 MDA14	
AK40 MDA15	
AM40 MDA17	
AM39 MDA21	
AP38 MDA18	
AP39 MDA19	
AM37 MDA20	
AM38 MDA16	
AP37 MDA22	
AP40 MDA23	
AV37 MDA25	
AW37 MDA29	
AU35 MDA26	
AT37 MDA27	
AU35 MDA28	
AU37 MDA24	
AU37 MDA30	
AW35 MDA31	
AY6 MDA33	
AU6 MDA37	
AV4 MDA34	
AU4 MDA35	
AW6 MDA36	
AW4 MDA38	
AY4 MDA39	
AR1 MDA41	
AR4 MDA45	
AN3 MDA42	
AN4 MDA43	
AR2 MDA44	
AR3 MDA40	
AN2 MDA46	
AN1 MDA47	
AL1 MDA49	
AL4 MDA53	
AJ3 MDA50	
AJ4 MDA51	
AL2 MDA52	
AJ2 MDA54	
AJ1 MDA55	
AG1 MDA57	
AG4 MDA61	
AE3 MDA58	
AE4 MDA59	
AG2 MDA60	
AG3 MDA56	
AE2 MDA62	
AE1 MDA63	
AE39 DOSA0	
AJ39 DOSA1	
AN39 DOSA2	
AV36 DOSA3	
AV5 DOSA4	
AP3 DOSA5	
AK3 DOSA6	
AE3 DOSA7	
AV32 -DQSA0	
AE38 -DQSA1	
AJ38 -DQSA2	
AN38 -DQSA3	
AU36 -DQSA4	
AW5 -DQSA5	
AP2 -DQSA6	
AK2 -DQSA7	
AF2 -DQSA7	
AU32	

HASWELL[10SC1-F01150-01R\_10SC1-F01150-03R]

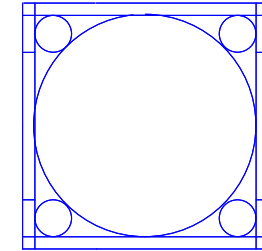
## LGA1150 (B)

LGA1150B	
MAAB0 AL19	DDR1_MA0
MAAB1 AM23	DDR1_MA1
MAAB2 AM23	DDR1_MA2
MAAB3 AM23	DDR1_MA3
MAAB4 AP23	DDR1_MA4
MAAB5 AL23	DDR1_MA5
MAAB6 AY24	DDR1_MA6
MAAB7 AV25	DDR1_MA7
MAAB8 AU26	DDR1_MA8
MAAB9 AW25	DDR1_MA9
MAAB10 AP18	DDR1_MA10
MAAB11 AY25	DDR1_MA11
MAAB12 AV26	DDR1_MA12
MAAB13 AR15	DDR1_MA13
AV27	DDR1_MA14
AY28	DDR1_MA15
MODT_B0 AM17	DDR1_ODT0
MODT_B1 AL16	DDR1_ODT1
MODT_B2 AM16	DDR1_ODT2
MODT_B3 AK15	DDR1_ODT3
AM26	DDR1_ECC0
AM25	DDR1_ECC1
AP25	DDR1_ECC2
AP26	DDR1_ECC3
AL26	DDR1_ECC4
AL25	DDR1_ECC5
AR26	DDR1_ECC6
AE25	DDR1_ECC7
SBA00 SBA01 AK17	DDR1_BA0
SBA01 SBA01 AL18	DDR1_BA1
SBA02 SBA02 AW28	DDR1_BA2
CKEB0 CKEB1 AW29	DDR1_CKE0
CKEB1 CKEB2 AU28	DDR1_CKE1
CKEB2 CKEB3 AU29	DDR1_CKE2
CSE0 CSB0 AP17	DDR1_CS_N0
CSB1 CSB1 AN15	DDR1_CS_N1
CSB2 CSB2 AN17	DDR1_CS_N2
CSB3 CSB3 AL15	DDR1_CS_N3
DCLKB0 DCLKB0 AM20	DDR1_CLK_P0
DCLKB0 DCLKB1 AM21	DDR1_CLK_N0
DCLKB1 DCLKB1 AP22	DDR1_CLK_P1
DCLKB1 DCLKB1 AP22	DDR1_CLK_N1
DCLKB2 DCLKB2 AN20	DDR1_CLK_P2
DCLKB2 DCLKB3 AP19	DDR1_CLK_N2
DCLKB3 DCLKB3 AP20	DDR1_CLK_P3
-DCLKB3 -DCLKB3	DDR1_CLK_N3
-SCASB -SCASB AP16C	DDR1_CAS*
-SRASB -SRASB AM18C	RSVD
-SWEB -SWEB AK16C	DDR1_RAS*
AB39	DDR1_WE*
AB40	
DDR_VREF_DQ0	
DDR_VREF_DQ1	
DOS_P0	
DOS_P1	
DOS_P2	
DOS_P3	
DOS_P4	
DOS_P5	
DOS_P6	
DOS_P7	
DOS_P8	
DOS_N0	
DOS_N1	
DOS_N2	
DOS_N3	
DOS_N4	
DOS_N5	
DOS_N6	
DOS_N7	
DOS_N8	
AE34 MDB0	
AE35 MDB1	
AG35 MDB2	
AH35 MDB3	
AD34 MDB4	
AD35 MDB5	
AG34 MDB6	
AH34 MDB7	
AL34 MDB8	
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AK32 MDB14	
AL32 MDB15	
AN34 MDB17	
AP34 MDB21	
AN31 MDB19	
AP31 MDB23	
AN35 MDB20	
AP35 MDB16	
AN32 MDB18	
AP32 MDB22	
AM29 MDB25	
AM28 MDB28	
AR29 MDB27	
AR28 MDB30	
AL29 MDB24	
AL28 MDB29	
AP29 MDB26	
AP28 MDB31	
AR12 MDB32	
AP12 MDB33	
AL13 MDB34	
AL12 MDB35	
AR13 MDB36	
AP13 MDB37	
AM13 MDB38	
AM12 MDB39	
AR9 MDB45	
AP9 MDB41	
AR6 MDB47	
AP6 MDB43	
AR10 MDB44	
AP10 MDB40	
AR7 MDB46	
AP7 MDB42	
AM9 MDB52	
AL9 MDB53	
AL6 MDB50	
AL6 MDB55	
AM10 MDB48	
AL10 MDB49	
AM6 MDB54	
AM7 MDB51	
AH6 MDB61	
AH7 MDB60	
AE6 MDB59	
AE7 MDB63	
AJ6 MDB56	
AJ7 MDB57	
AF6 MDB58	
AF7 MDB62	
AE35 DOSB0	
AL33 DOSB1	
AN28 DOSB2	
AN28 DOSB3	
AN12 DOSB4	
AP8 DOSB5	
AL8 DOSB6	
AG7 DOSB7	
AN24 -DQSB0	
AK33 -DQSB1	
AN33 -DQSB2	
AK33 -DQSB3	
AN29 -DQSB4	
AR13 -DQSB5	
AR8 -DQSB6	
AG6 -DQSB7	
AN29	



HASWELL[10SC1-F01150-01R\_10SC1-F01150-03R]

## LGA1150 (CR)

LGA1150  
ILM\_BP/1156/BKNI/12KRC-0F0001-52R\_12KRC-0F0001-51R

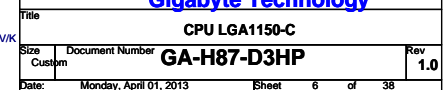
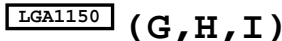
## DDR BUS

7 MODT_A[0..3]	MODT_A[0..3]
8 MODT_B[0..3]	MODT_B[0..3]
7 MDA[0..63]	MDA[0..63]
8 MDB[0..63]	MDB[0..63]
7 DQSA[0..7]	DQSA[0..7]
7 -DQSA[0..7]	-DQSA[0..7]
7 MAA[0..15]	MAA[0..15]
8 MAAB[0..15]	MAAB[0..15]
8 DQSB[0..7]	DQSB[0..7]
8 -DQSB[0..7]	-DQSB[0..7]

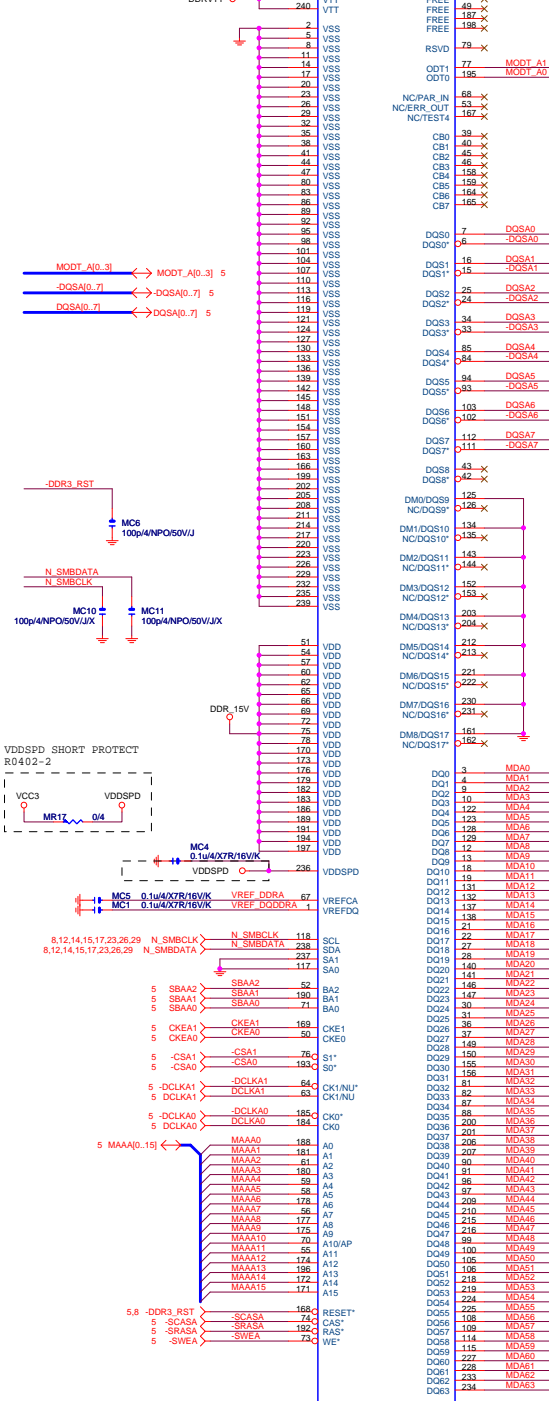
## Gigabyte Technology

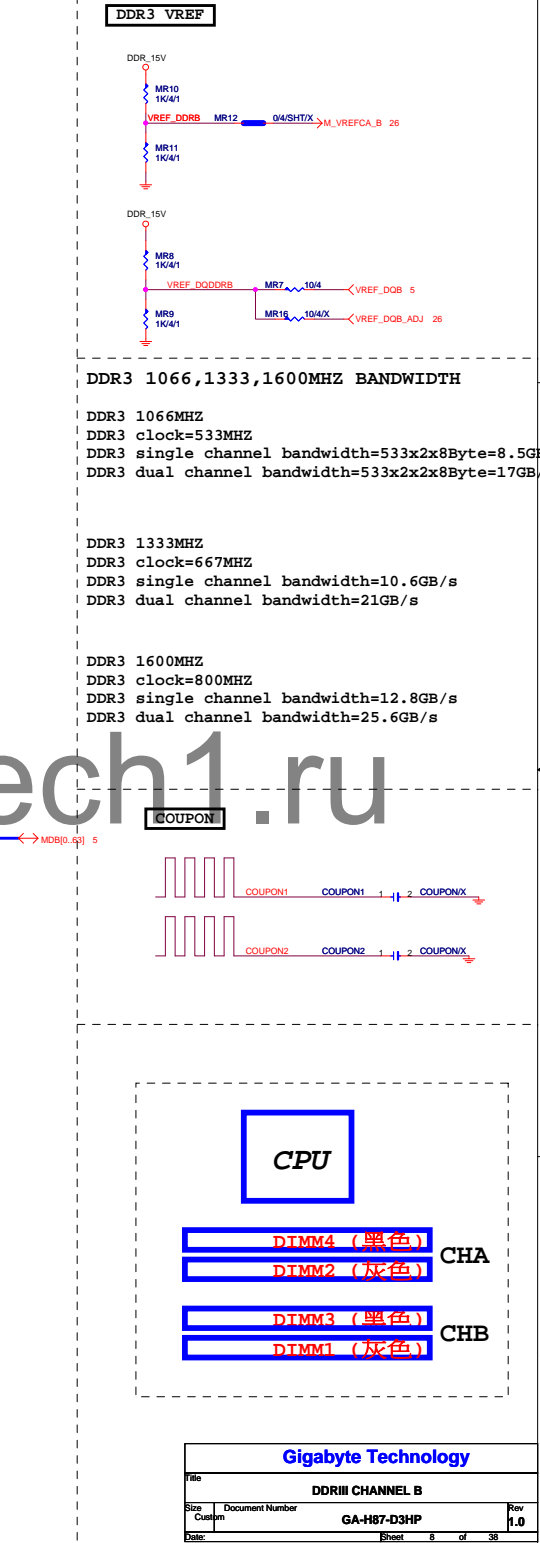
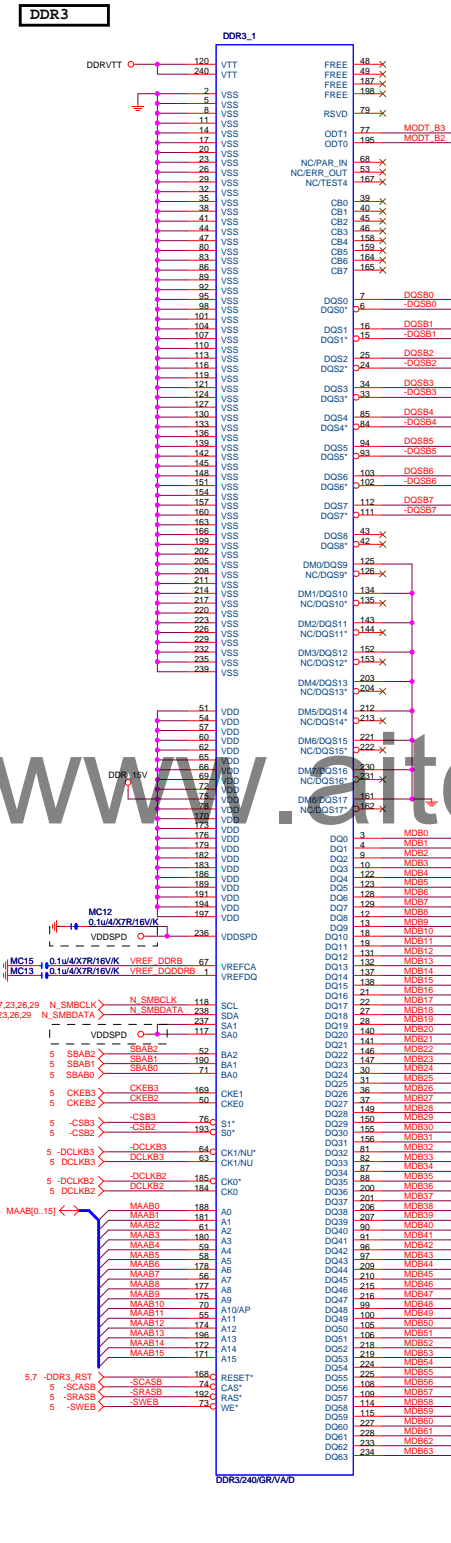
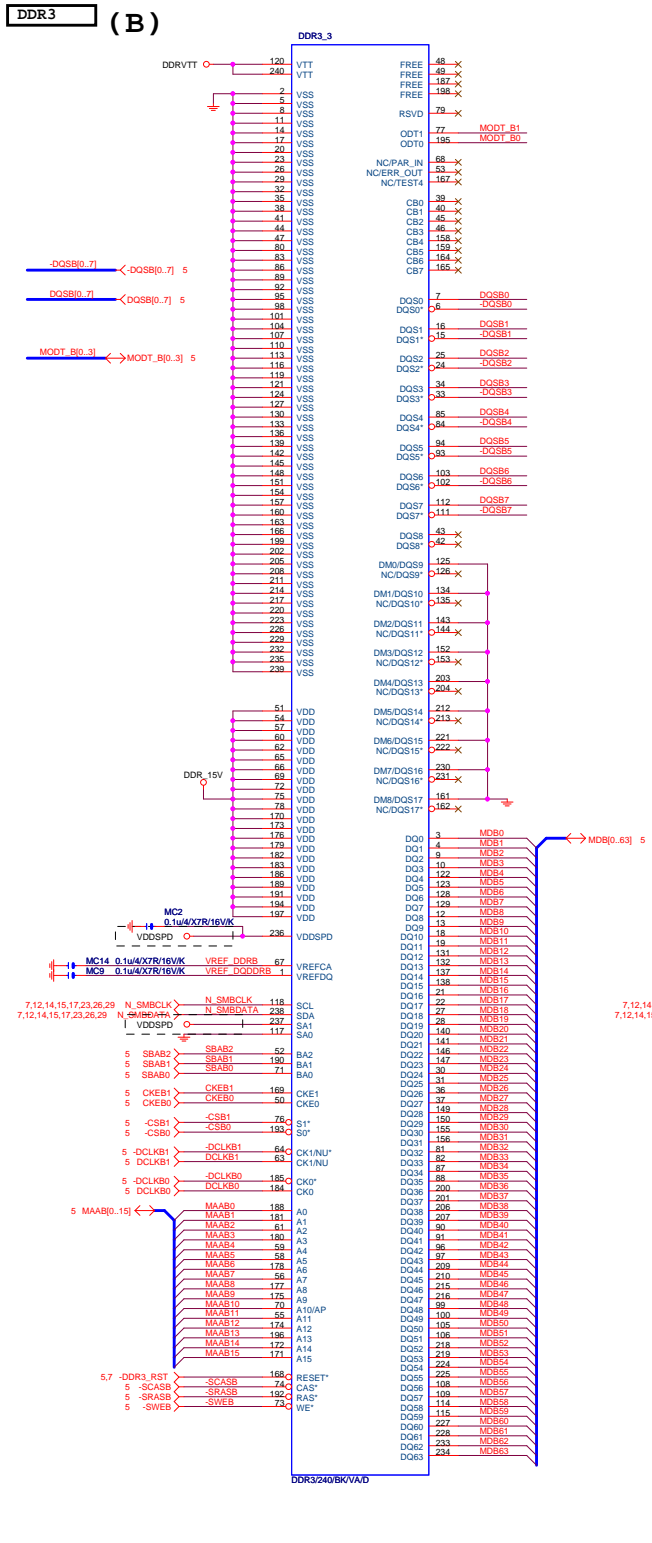
Title			
CPU LGA1150-B			
Size	Document Number	Rev	
Custom	GA-H87-D3HP	1.0	
Date:	Monday, April 01, 2013	Sheet	5 of 38

(F, J)



# DDR3 (A)





# PCH (B)

DMI:12/4/4/12(breakout min 8/4/4/4/8)  
Impedance=85 +- 17.5%

USB2.0 : 12/5/7/5/12 (breakout min 8/4/4/4/8)  
Impedance=85 +- 17.5%

4 A DMI\_0TXN A DMI\_0TXP L24  
4 A DMI\_0TXN A DMI\_0TXP K24  
4 A DMI\_0RXN A DMI\_0RXP C20  
4 A DMI\_0RXN A DMI\_0RXP B20  
4 A DMI\_1TXN A DMI\_1TXN G24  
4 A DMI\_1TXN A DMI\_1TXN H24  
4 A DMI\_1TXN A DMI\_1RXN D24  
4 A DMI\_1RXN A DMI\_1RXN B21  
4 A DMI\_1TXN A DMI\_1TXN F26  
4 A DMI\_2TXN A DMI\_2TXN G26  
4 A DMI\_2TXN A DMI\_2TXN B22  
4 A DMI\_2RXN A DMI\_2RXN C22  
4 A DMI\_2RXN A DMI\_2TXN K26  
4 A DMI\_3TXN A DMI\_3TXN L26  
4 A DMI\_3TXN A DMI\_3RXN A24  
4 A DMI\_3RXN A DMI\_3RXN B24  
4 A DMI\_3RXN A DMI\_3RXN B24

VCC1\_5\_PCH NR50 7.5K/4/1 DMI\_COMP B19  
W=8 mil out of PCH NR40 7.5K/4/1 PCIE\_COMP C13  
S=15 mil to other signals  
ITE8892 PCI CK-SRCLK\_PCH CK-SRCLK\_PCH G22  
CK-SRCLK\_PCH CK-SRCLK\_PCH F22

Bridge  
PCIEX1 port1 15 PI\_PCIE\_IN1 L14  
15 PI\_PCIE\_IP1 K14  
15 PI\_PCIE\_TP1 B12  
15 PI\_PCIE\_TP1 B11  
15 PJ\_PCIE\_IN2 F14  
15 PJ\_PCIE\_IP2 D11  
15 PJ\_PCIE\_TP2 C11  
15 PJ\_PCIE\_TP2 F11  
LAN AR8161 31 LB\_ML\_IN H11  
31 LB\_ML\_IP B9  
31 LB\_ML\_ON A9  
31 LB\_ML\_OP J11  
16 G\_PCIEBIN L11  
16 G\_PCIEBIP B8  
16 G\_PCIEBON C8  
16 G\_PCIEBOP G9  
PCIEX4 port1 15 PE\_PCIE\_IN1 E9  
15 PE\_PCIE\_IP1 E7  
15 PE\_PCIE\_TP1 A7  
15 PE\_PCIE\_TP1 F7  
15 PF\_PCIE\_IN2 H7  
15 PF\_PCIE\_IP2 D2  
15 PF\_PCIE\_TP2 K6  
15 PG\_PCIE\_IN3 K8  
15 PG\_PCIE\_IP3 G3  
15 PG\_PCIE\_TP3 G5  
15 PH\_PCIE\_IN4 J3  
15 PH\_PCIE\_IP4 H2  
15 PH\_PCIE\_TP4 H1

電容放靠近 Device & PCI-E Slot

PCIEX1:15/4/4/15 (breakout min 8/4/4/4/8)  
Impedance=85 +- 17.5%

PCH\_PCIE, DMI 15/4/4/4/15

usb2.0 12/5/7/5/12

usb3.0 20/5/7/5/20

# PCH (F)

USB3.0 : 20/5/7/5/20 (breakout min 8/4/4/4/8)  
Impedance=85 +- 17.5%

28 PCH\_USB3\_RXN0 F20  
28 PCH\_USB3\_RXP0 G20  
28 PCH\_USB3\_TXN0 B18  
28 PCH\_USB3\_TXP0 C18  
28 PCH\_USB3\_RXN1 G18  
28 PCH\_USB3\_RXP1 H18  
28 PCH\_USB3\_TXN1 B15  
28 PCH\_USB3\_TXP1 B16  
34 PCH\_USB3\_RXN4 K20  
34 PCH\_USB3\_RXP4 L20  
34 PCH\_USB3\_TXN4 D15  
34 PCH\_USB3\_TXP4 C15  
36 PCH\_USB3\_RXN5 L18  
36 PCH\_USB3\_RXP5 K18  
36 PCH\_USB3\_TXN5 B14  
36 PCH\_USB3\_TXP5 A14

VCC3 NR62 8.2K/4  
NR63 8.2K/4 AK28  
AT34

FDI\_TXP0..1 FDI\_TXP0..1 4  
FDI\_TXN0..1 FDI\_TXN0..1 4

USB3.0:20/5/7/5/20 (breakout min 8/4/4/4/8) ; ONLY 3 VIAS  
Impedance=85 +- 17.5%  
Back Panel < 10000 MILS  
Front Panel < 6000 MILS

Mount for integrated clock Generation Mode

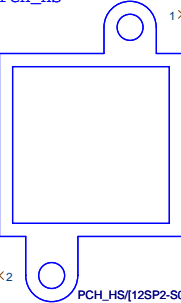
CK\_DOTCLK NR92 8.2K/4  
CK\_DOTCLK NR91 8.2K/4  
NR92 short to GND in non graphic SKU

# PCH (J)

AT1 VSS\_NCTF TP22 U11  
AT41 VSS\_NCTF TP23 U10  
AU1 VSS\_NCTF TP21 AJ14  
AV1 VSS\_NCTF TP20 AK14  
AV2 VSS\_NCTF TP14 K34  
AV41 VSS\_NCTF TP15 K33  
AW2 VSS\_NCTF TP12 AH24  
AW40 VSS\_NCTF TP10 L16  
B40 VSS\_NCTF TP11 K16  
B41 VSS\_NCTF TP9 AM34  
C41 VSS\_NCTF TP3 R12  
D1 VSS\_NCTF TP4 N12  
D41 VSS\_NCTF TP1 L22  
TP2 K22  
TP5 K5  
TP6 K5  
TP7 P5  
TP8 L5  
VSS AC31  
VSS AF3  
VSS AV21

# PCH H/S

PCH\_HS



PCH\_HS[12SP2-S06012-11R\_12SP2-S06012-12R\_12SP2-S06012-13R]

# USB TABLE

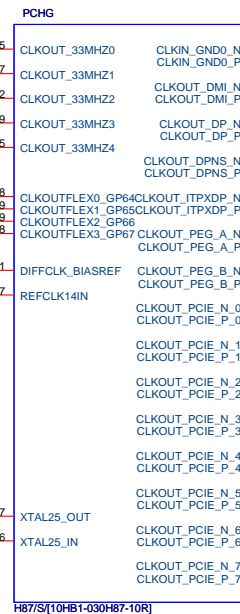
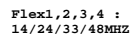
OC[3:0]# for Device 29 (ports 0-7)  
OC[7:4]# for Device 26 (ports 8-13)

USB OC# Configure	
OC0#	USB0,1
OC1#	USB2,3
OC2#	USB4,5
OC3#	USB6,7
OC4#	USB8,9
OC5#	USB10,11
OC6#	USB12,13
OC7#	Not Use

# Gigabyte Technology

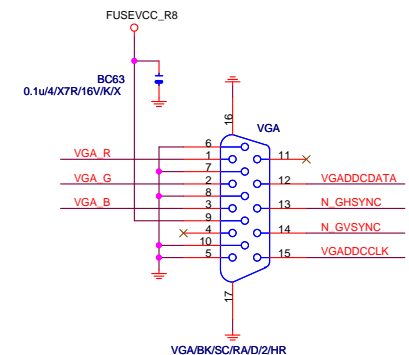
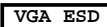
Title PCH FDI,DMI,USB ,PCIE		
Size Custom	Document Number GA-H87-D3HP	Rev 1.0
Date: Monday, April 01, 2013	Sheet 9	of 38

**PCH (G)**



Differential Clock:15/4/6/4/15  
Impedance=90 +- 15%

PCH CLK PD
------------



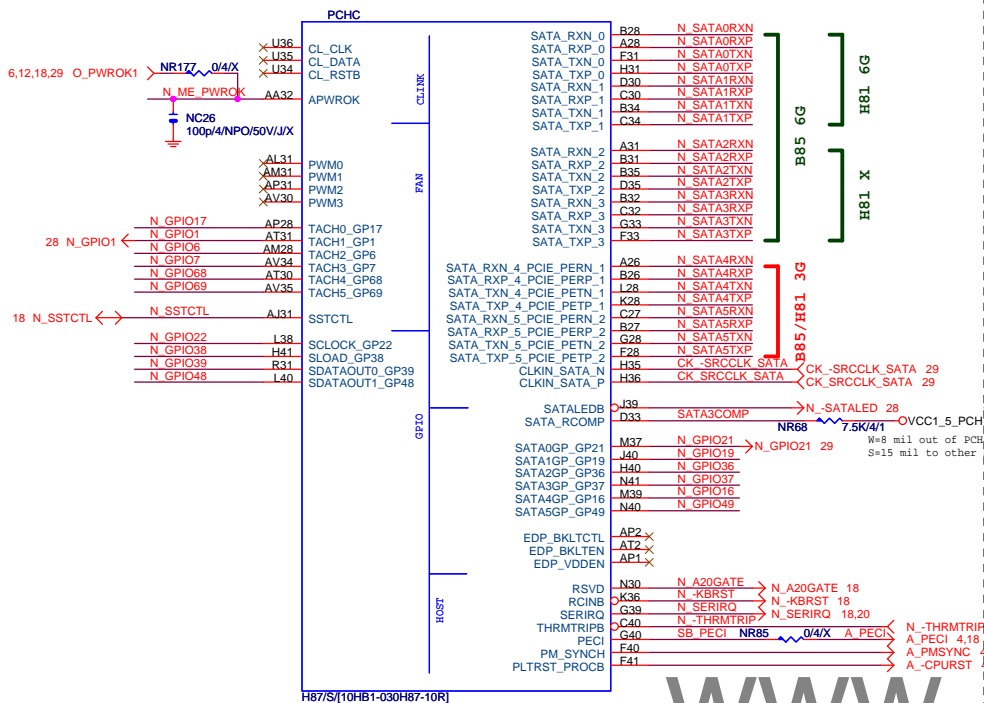
## Gigabyte Technology

Title	PCH DISPLAY ,CLK BUFFER
-------	-------------------------

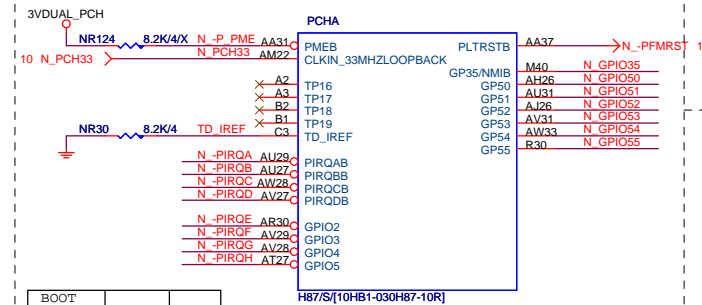
Size Custom	Document Number <b>GA-H87-D3HP</b>	Rev 1.0
Date: Monday, April 01, 2013	Sheet 10 of 38	

(C)

SATA3 : 20/4/4/4/20 (breakout min 8/4/4/4/8)  
Impedance=85 +- 17.5%



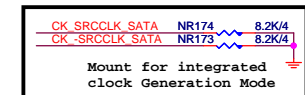
**PCH (A)**



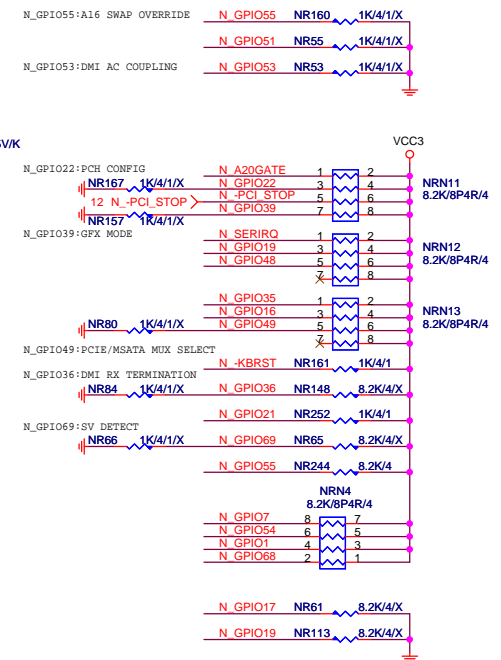
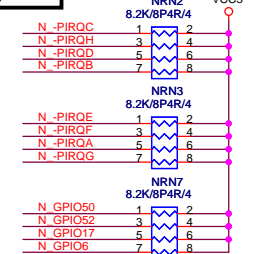
BOOT DEVICE	GP51	GP19
LPC	0	0
SPI	1	1

```
Default int pull up on GP51,  
Default SPI boot devices
```

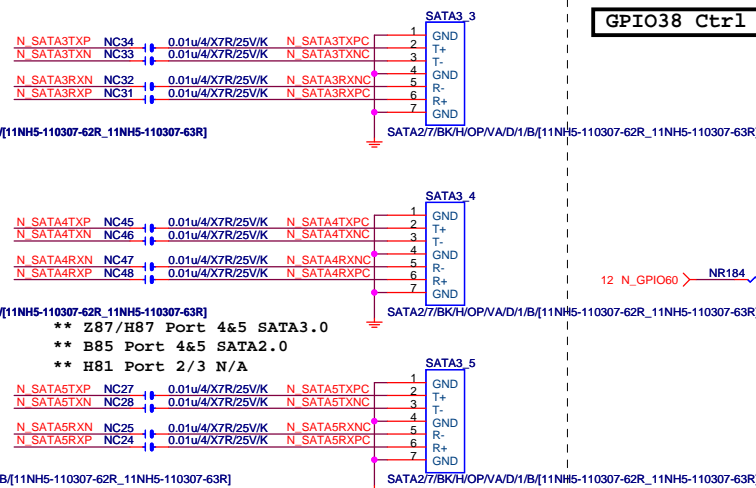
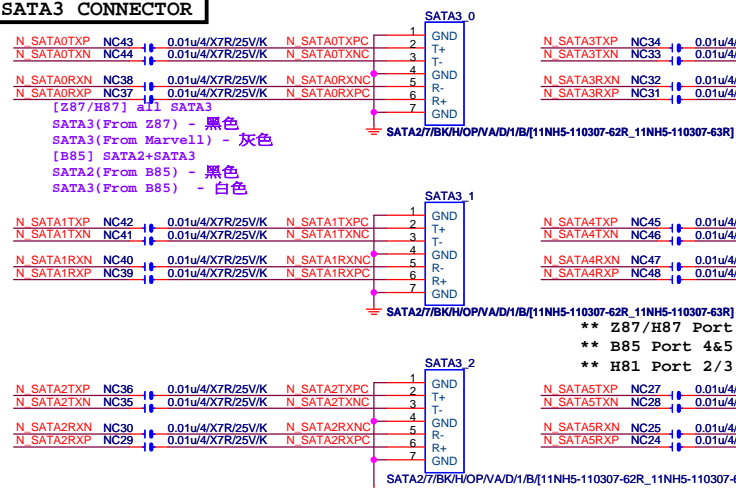
PCH CLK PD



PCH PU/PD



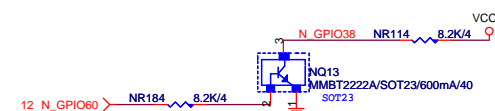
### SATA3 CONNECTOR



GPIO38 Ctrl

MFG Mode

```
N_GPIO38 : Lo --> Enable
           Hi --> Disable
```

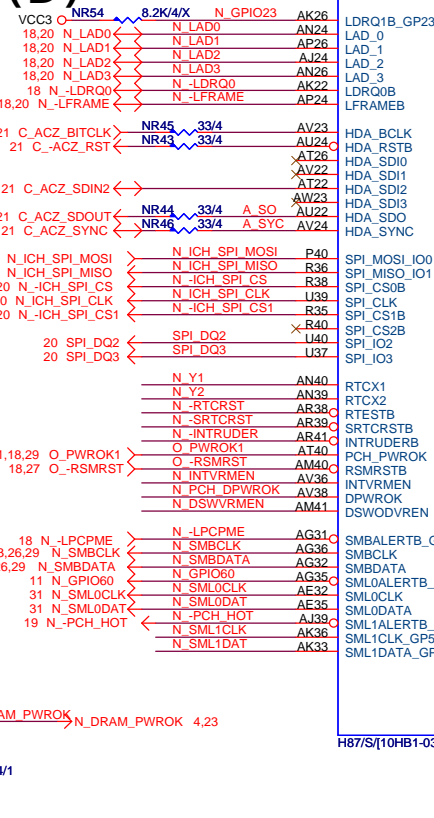


## Gigabyte Technology

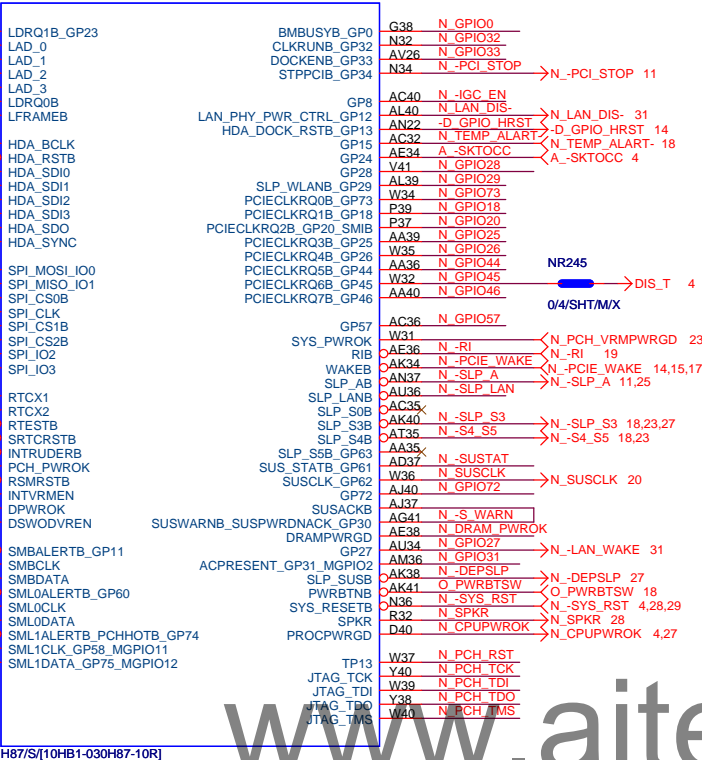
Title			
PCH HOST , SATA, PCI			
Size	Document Number		Rev
Custom	GA-H87-D3HP		1.0
Date:	Monday, April 01, 2013	Sheet	11 of 38

# PCH

(D)



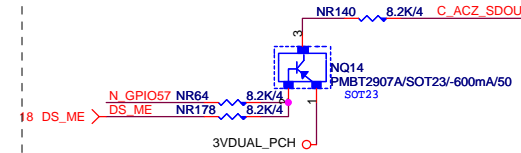
## PCHD



## ACZ\_SDOUT

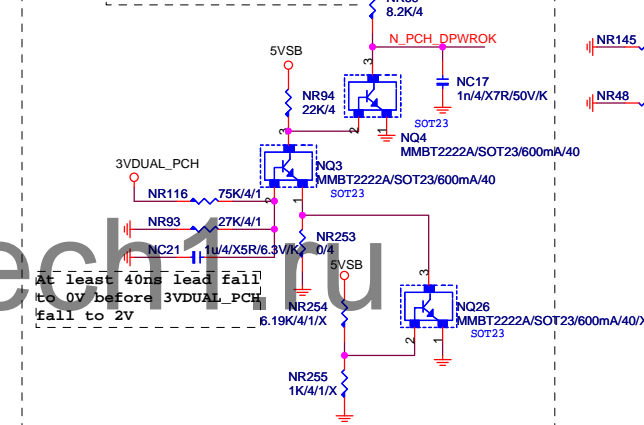
SPI OVERRIDE PROTECTION

C\_ACZ\_SDOUT : HI --> ME Enable  
Lo --> ME Disable

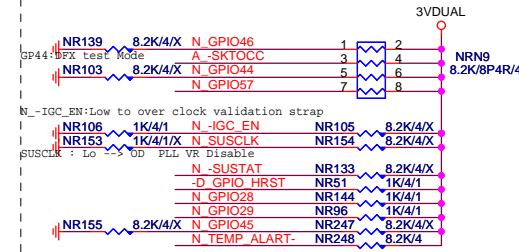


## PCH\_DPWROK

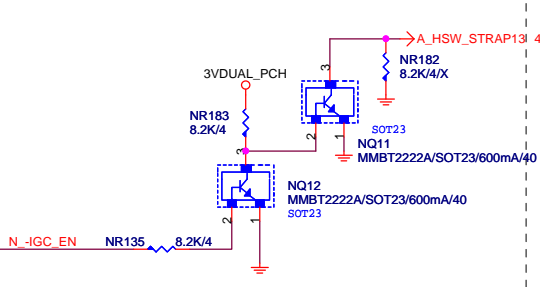
At least 10ms delay after 3VDUAL\_PCH stable



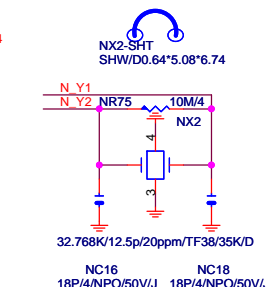
## PCH PU/PD



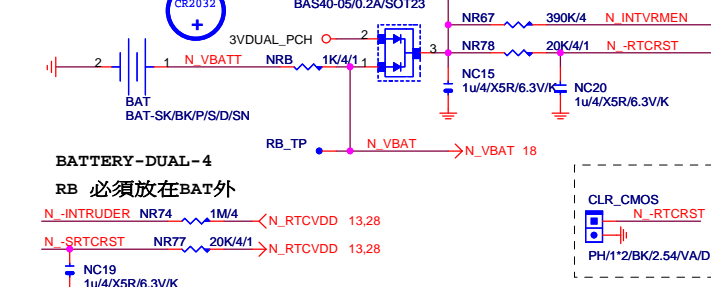
## HSW\_STRAP13



## 32.768KHZ



## CLR\_CMOS

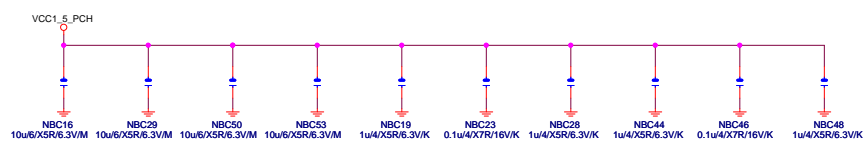


Gigabyte Technology			
PCH GPIO , CTRL , AUDIO			
Title	Document Number	Rev	1.0
Size	Custom	GA-H87-D3HP	
Date:	Monday, April 01, 2013	Sheet	12 of 38

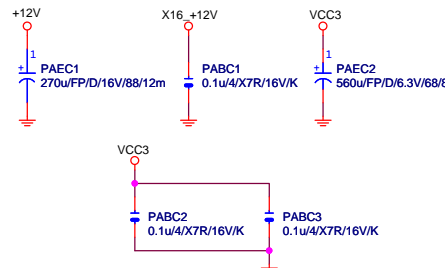
**PCH (I)**



SHT PWR

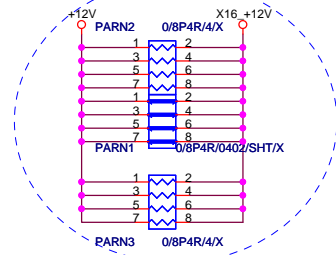


## PCIEX16 CAP



## PCIEX16 PROTECT SHT

```
+12 protect
short-wire test
```



## PCIEX16 AC CAP

PA EXP TXP0	PAC5	0.22u4/X5R6.3V/K	PA EXP TXP0 C
PA EXP TXP0	PAC4	0.22u4/X5R6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u4/X5R6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u4/X5R6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u4/X5R6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u4/X5R6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u4/X5R6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u4/X5R6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u4/X5R6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u4/X5R6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u4/X5R6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u4/X5R6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u4/X5R6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u4/X5R6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC19	0.22u4/X5R6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC18	0.22u4/X5R6.3V/K	PA EXP TXN7 C
PA EXP TXP8	PAC20	0.22u4/X5R6.3V/K	PA EXP TXP8 C
PA EXP TXN8	PAC21	0.22u4/X5R6.3V/K	PA EXP TXN8 C
PA EXP TXP9	PAC22	0.22u4/X5R6.3V/K	PA EXP TXP9 C
PA EXP TXN9	PAC23	0.22u4/X5R6.3V/K	PA EXP TXN9 C
PA EXP TXP10	PAC24	0.22u4/X5R6.3V/K	PA EXP TXP10 C
PA EXP TXN10	PAC25	0.22u4/X5R6.3V/K	PA EXP TXN10 C
PA EXP TXP11	PAC26	0.22u4/X5R6.3V/K	PA EXP TXP11 C
PA EXP TXN11	PAC27	0.22u4/X5R6.3V/K	PA EXP TXN11 C
PA EXP TXP12	PAC28	0.22u4/X5R6.3V/K	PA EXP TXP12 C
PA EXP TXN12	PAC29	0.22u4/X5R6.3V/K	PA EXP TXN12 C
PA EXP TXP13	PAC30	0.22u4/X5R6.3V/K	PA EXP TXP13 C
PA EXP TXN13	PAC31	0.22u4/X5R6.3V/K	PA EXP TXN13 C
PA EXP TXP14	PAC32	0.22u4/X5R6.3V/K	PA EXP TXP14 C
PA EXP TXN14	PAC33	0.22u4/X5R6.3V/K	PA EXP TXN14 C
PA EXP TXP15	PAC34	0.22u4/X5R6.3V/K	PA EXP TXP15 C
PA EXP TXN15	PAC35	0.22u4/X5R6.3V/K	PA EXP TXN15 C

PCI-E REV:1.1--&gt; 2.5GHZ

PCE-E X1(單向) BANDWIDTH=2.5GHz\*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWIDTH=2.5GHz\*(8b/10b)X2=4Gb/s±500MB/s

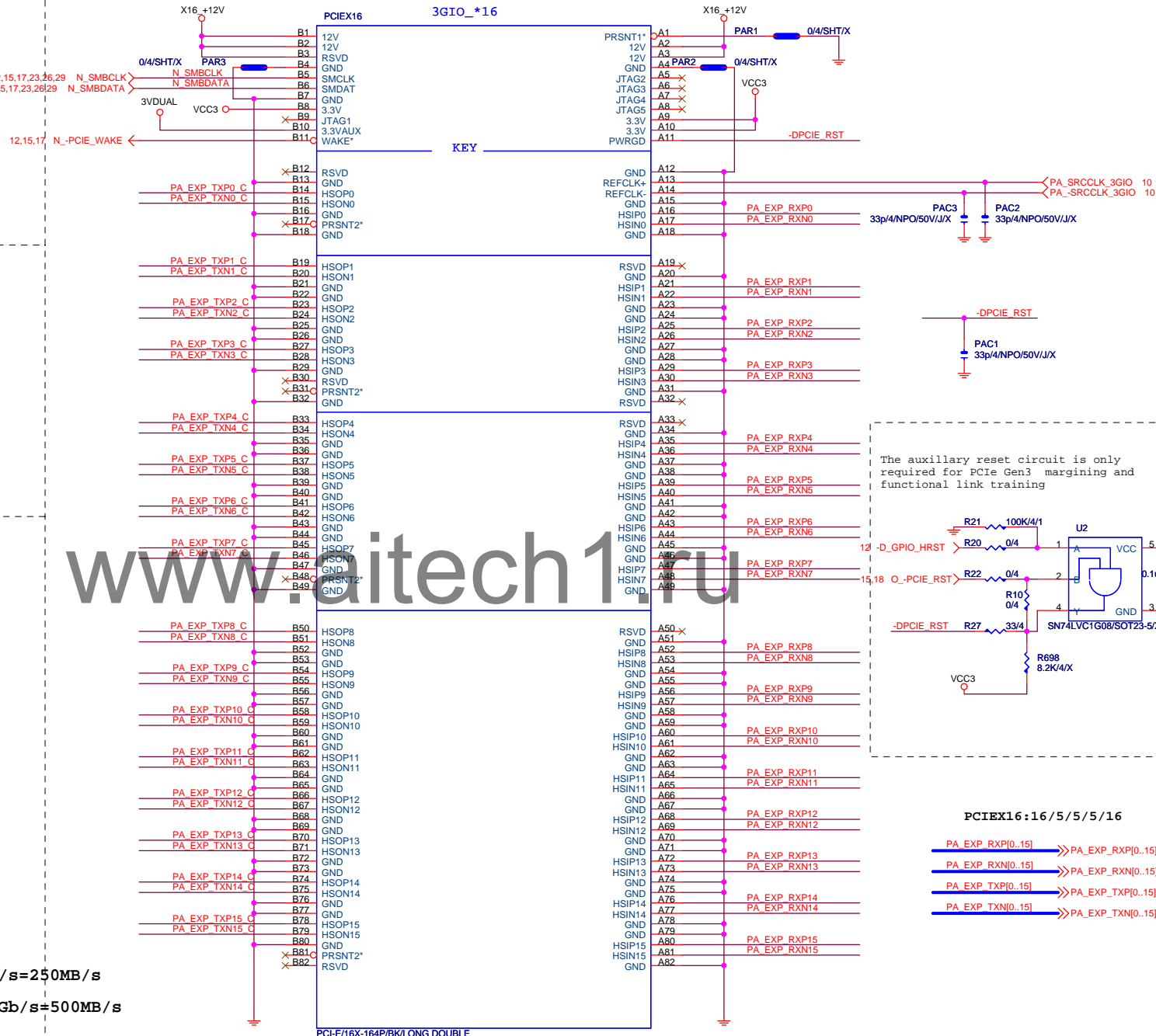
PCE-E X16(單向) BANDWIDTH=2.5GHz\*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWIDTH=2.5GHz\*(8b/10b)X16X2=64Gb/s=8GB/s

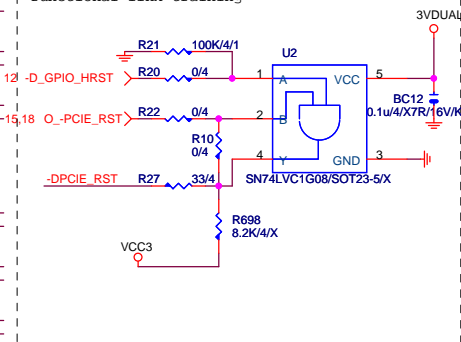
PCI-E REV:2.0--&gt; 5GHZ

PCIEX16 SLOT

PCIESLOT-164DN-Q

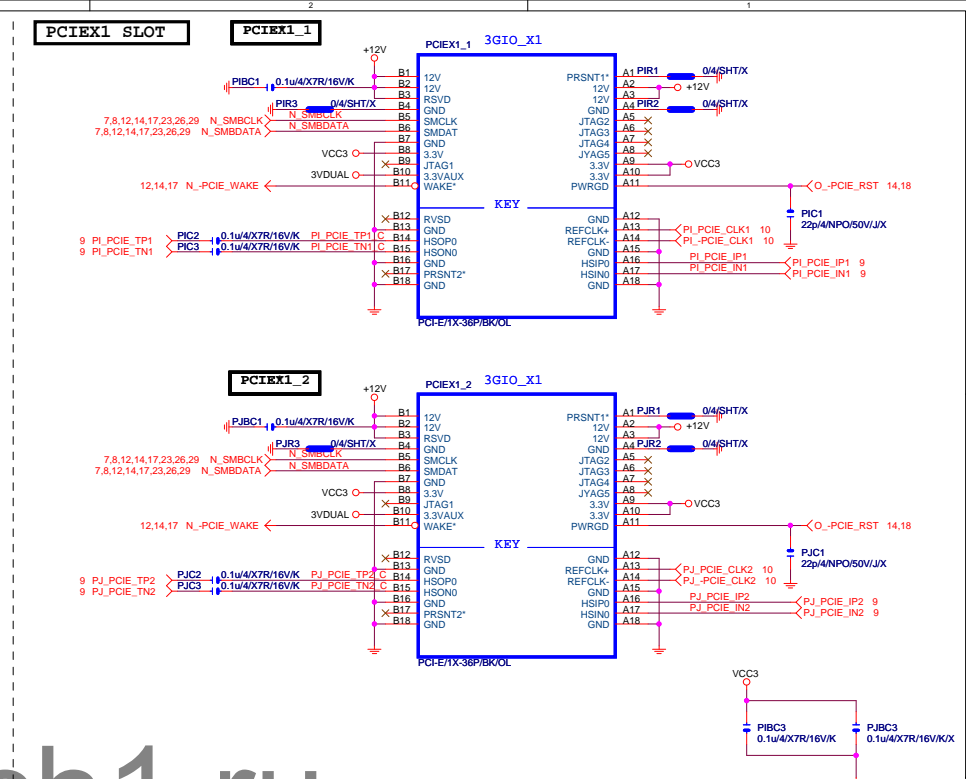
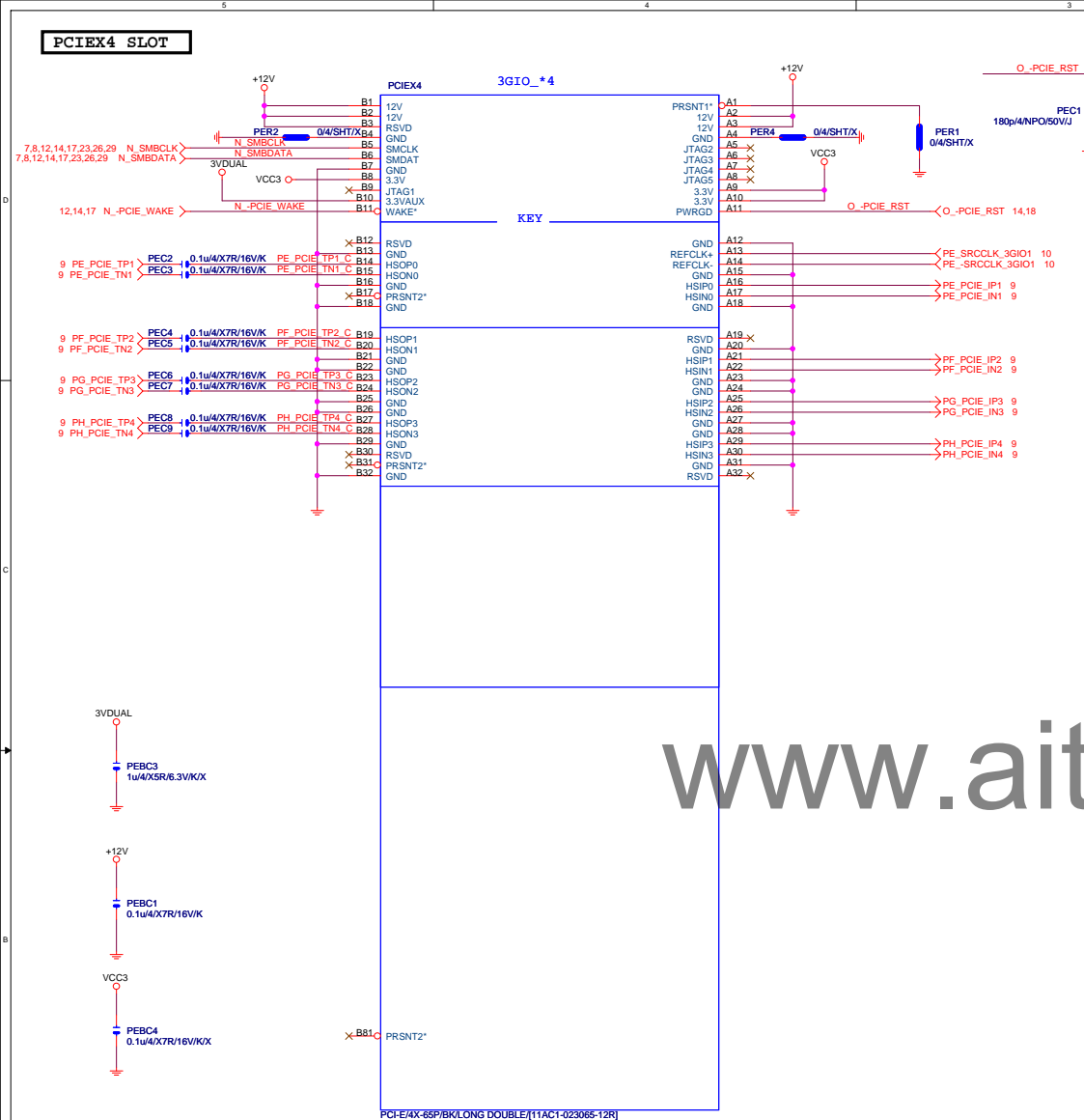


```
- | The auxillary reset circuit is only
| required for PCIe Gen3  margining and
- | functional link training
```



PCIEX16:16/5/5/5/16

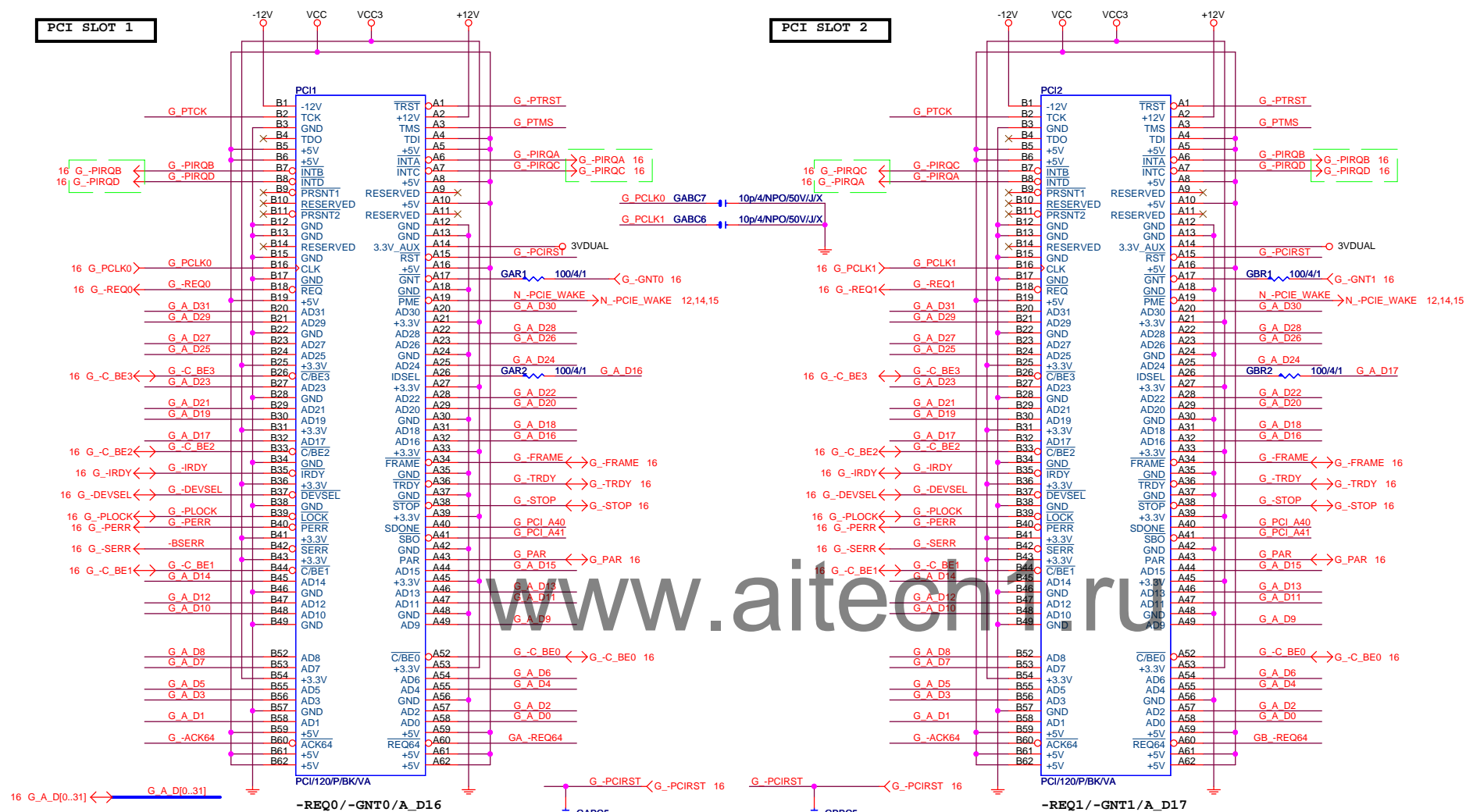
```
PA_EXP_RXP[0..15] >>> PA_EXP_RXP[0..15] 4
PA_EXP_RXN[0..15] >>> PA_EXP_RXN[0..15] 4
PA_EXP_TXP[0..15] >>> PA_EXP_TXP[0..15] 4
PA_EXP_TXN[0..15] >>> PA_EXP_TXN[0..15] 4
```





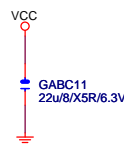
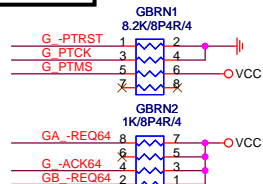
# PCI SLOT 1

# PCI SLOT 2



## PCI PU

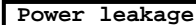
## PCI CAP



**GIGABYTE**

PCI SLOT 1&2		
Size	Document Number	Rev
Custom	<b>GA-H87-D3HP</b>	<b>1.0</b>
Date:	Monday, April 01, 2013	Sheet 17 of 38

## IT8728F NOTE

DUAL BIOS OPT STRAP

PWR	SHT
-----	-----

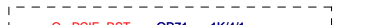
For 8728 EUP function



VCC3 **OR49** 0/6/SHT/X IT\_AVCC

DS\_ME OR46 1K/4/1 3VDUAL\_PCH

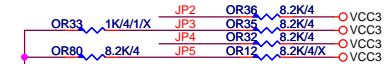
SVID\_CTRL OR84 8.2K/4 3VDUAL\_PCH



```
Hi :Disable WDT
Lo :Enable WDT to rest PWROK
```

2 SIO STRAP

```
-- High SPI-Flash Disable
   Low SPI-Flash Enable
```



JP5:N\A FOR 8728 DX  
JP5:PULL DOWN FOR 8728 EX  
anti-surge enable

```

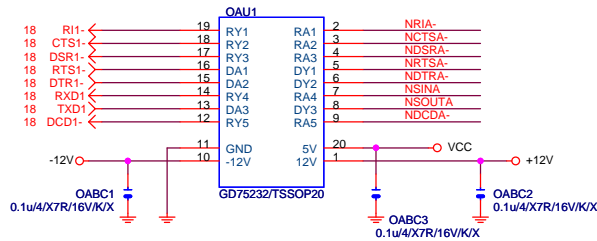
- - - - -
P control detect

```

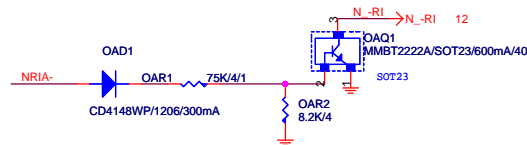


JP4	1	k8 power sequency function is Disable
	0	k8 power sequency function is Enable
JP3	1 1	The default value of EC Index 63h/6Bh/73h is 80h
	1 0	The default value of EC Index 63h/6Bh/73h is FFh
JP5	0 1	The default value of EC Index 63h/6Bh/73h is 00h
	0 0	The default value of EC Index 63h/6Bh/73h is 0Fh

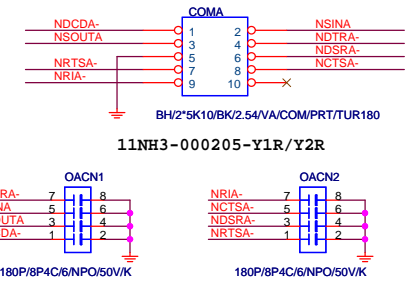
## COMA



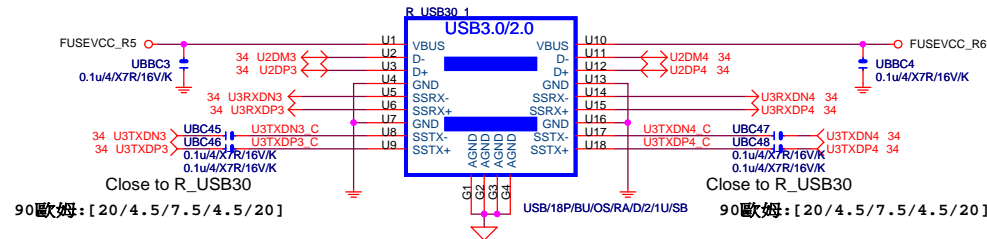
## COM RI



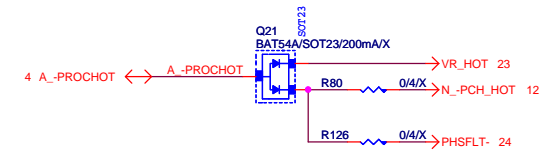
## COM BUFFER



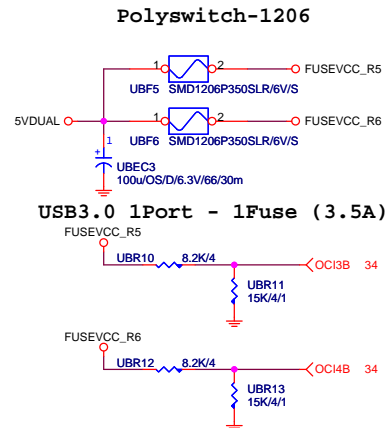
## USB30\_20 CONNECT



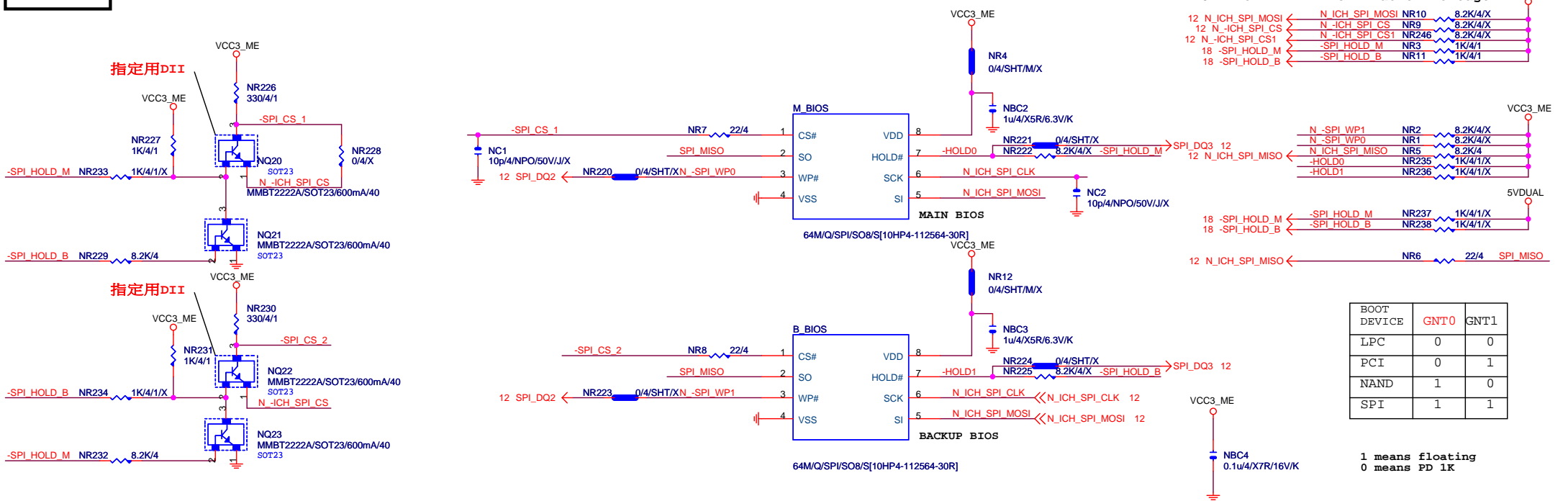
## -PROHOT



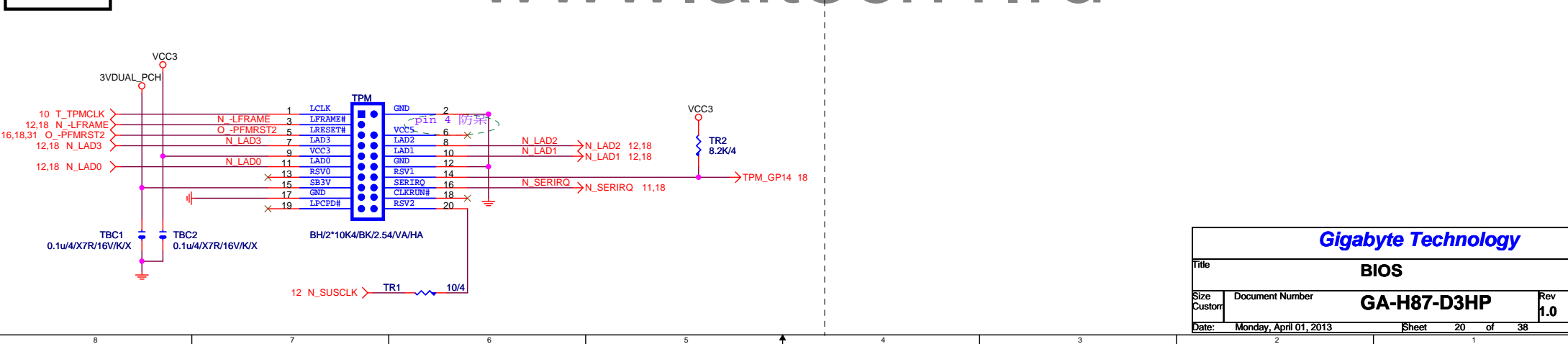
## USB30 PWR



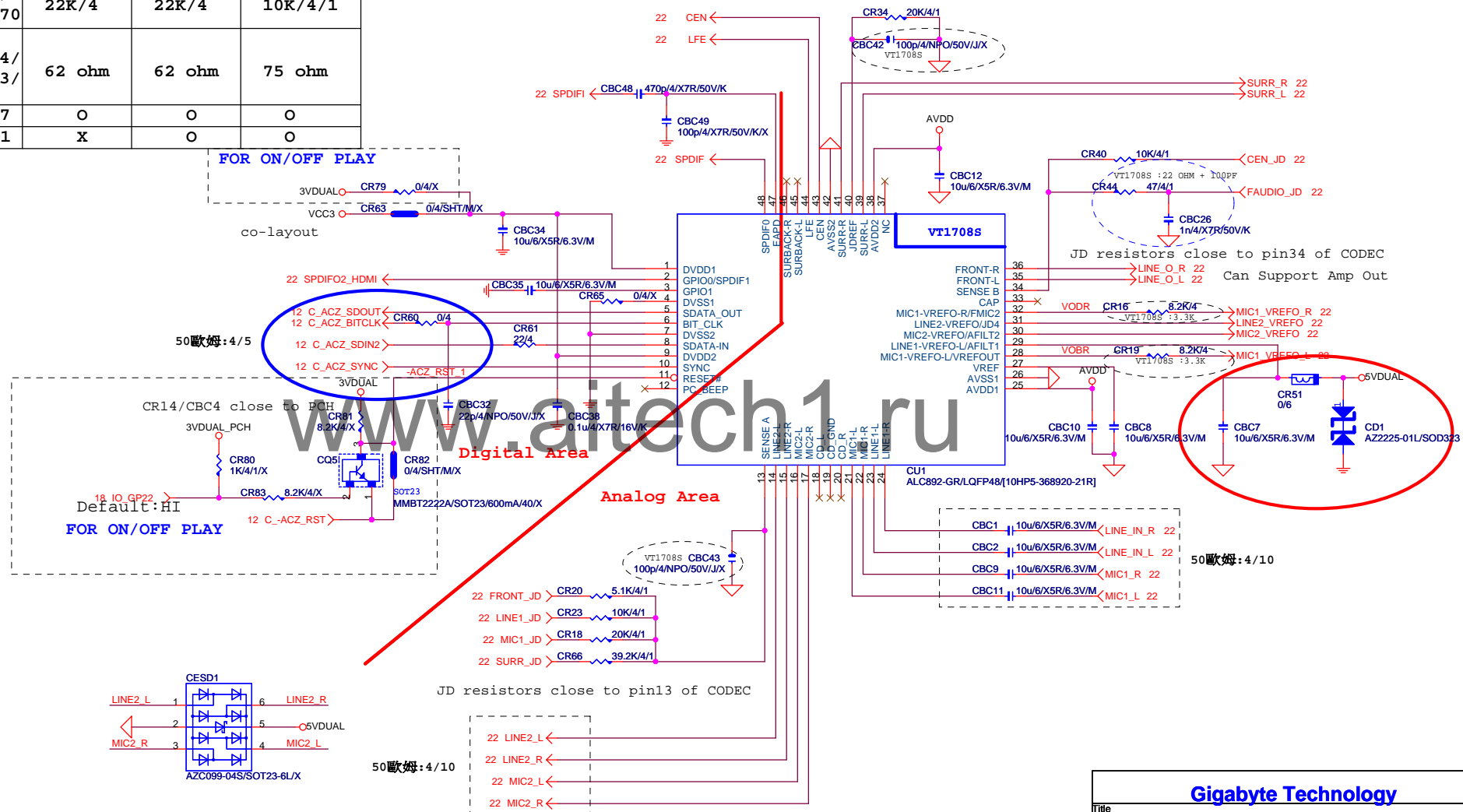
# DUAL BIOS

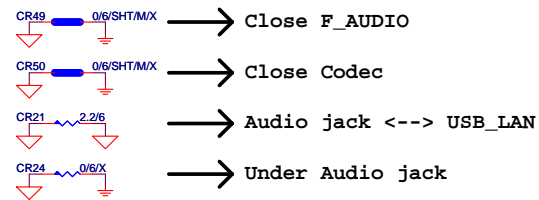


# TPM CONNECT

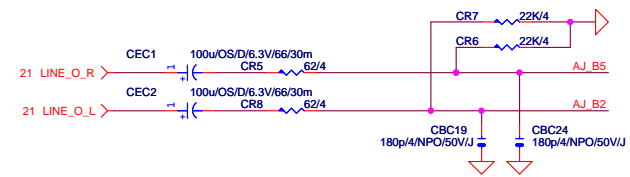


	ALC892	ALC887-VD2	VT1708S-CE
CR44/CBC26	47ohm+1nF	47ohm+1nF	22ohm+100P
CBC42/CBC43	X	X	100P/4
CR16/CR19 CR52/CR56/CR10/CR9	8.2K/4	8.2K/4	3.3K/4/1
CR6/CR7/CR58/CR54/ CR67/CR68/CR69/CR70	22K/4	22K/4	10K/4/1
CR5/CR8/CR1/CR14/ CR17/CR22/CR73/CR74/ CR13/CR11/CR57/CR53/ CR75/CR76	62 ohm	62 ohm	75 ohm
CR51/CD1/CBC7	O	O	O
CESD1	X	O	O





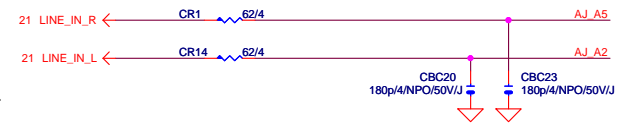
#### LINE-OUT



#### LINE-IN

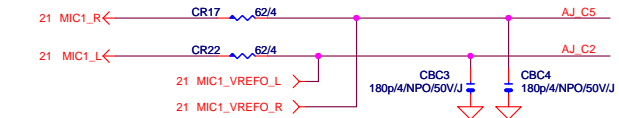
Verify MIC function  
in LINE-in

Only reserved for ALC888

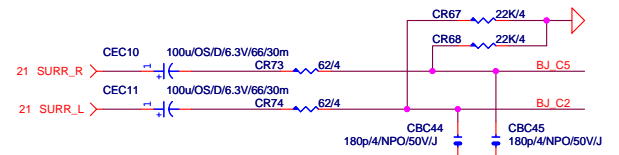


For 889A/888

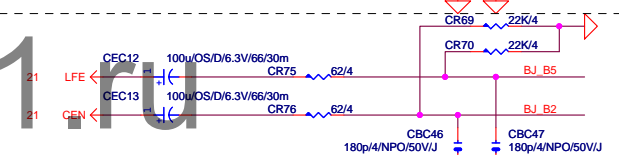
#### MIC-IN



#### SURROUND

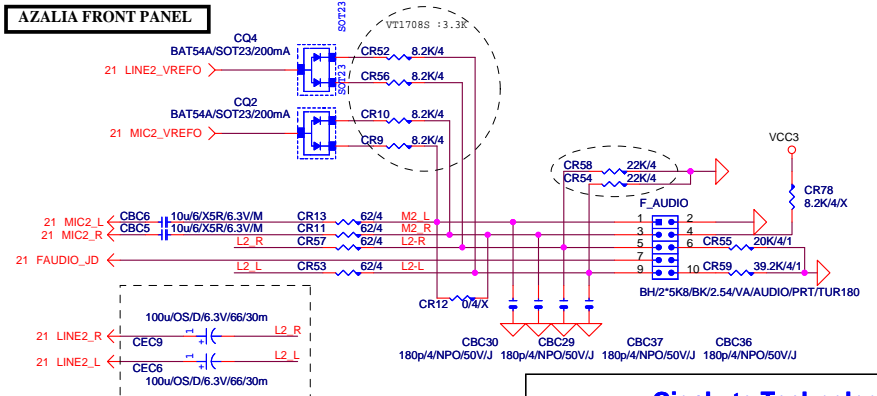


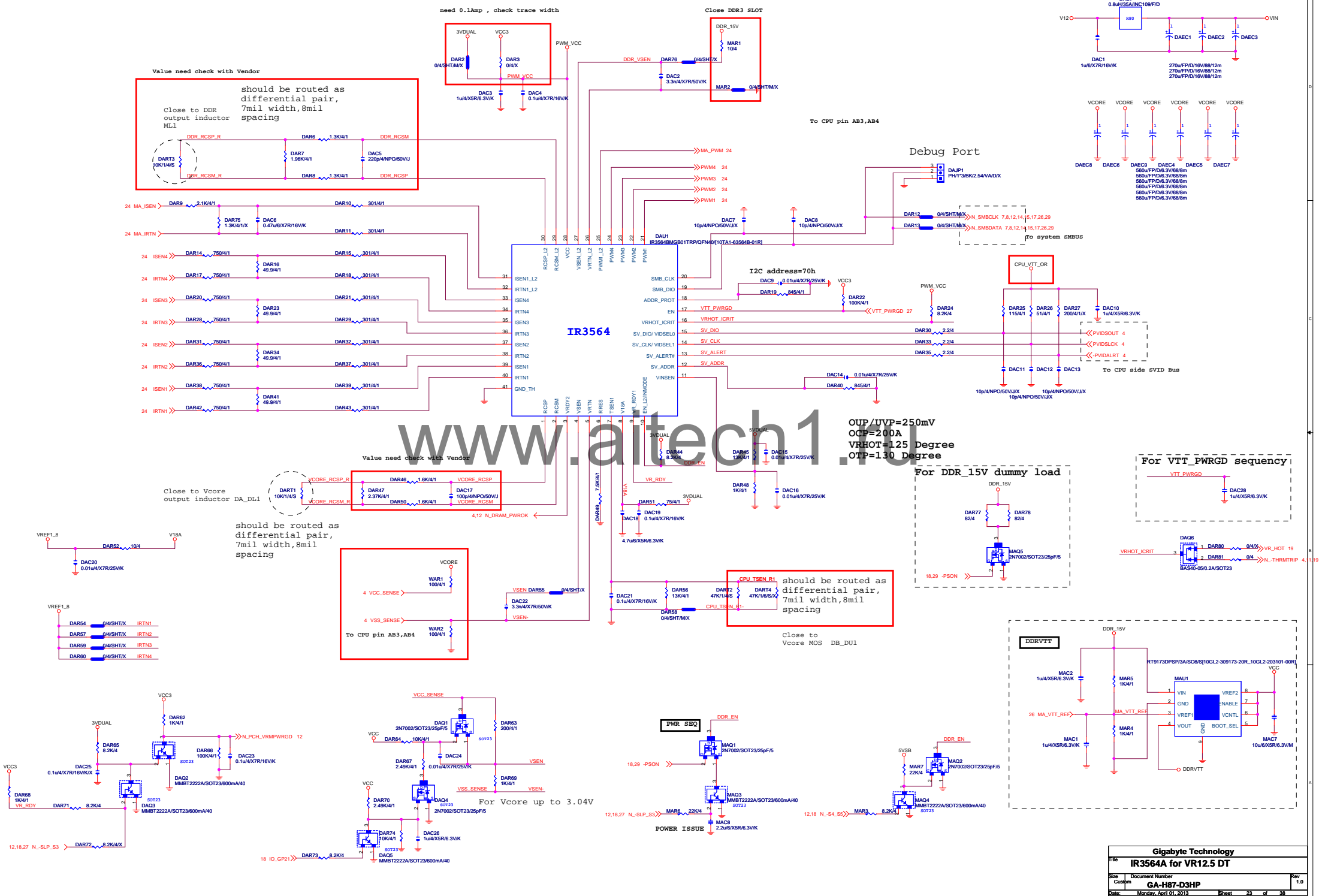
#### CEN/LFE



#### SURR BACK

#### AZALIA FRONT PANEL





Value need check with Vendor

should be routed as differential pair, 7mil width, 8mil spacing

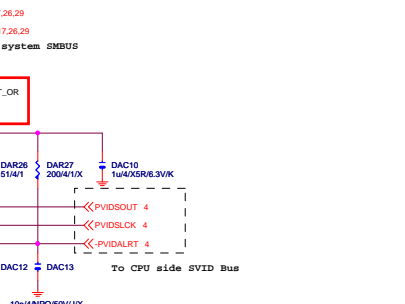
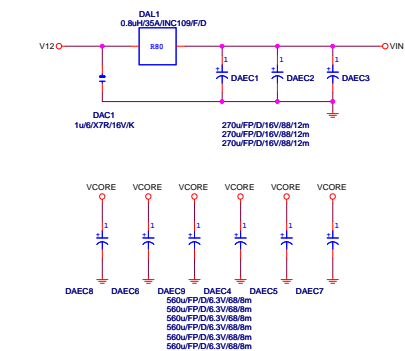
Close to DDR output inductor ML1

need 0.1amp, check trace width

Close DDR3 SLOT

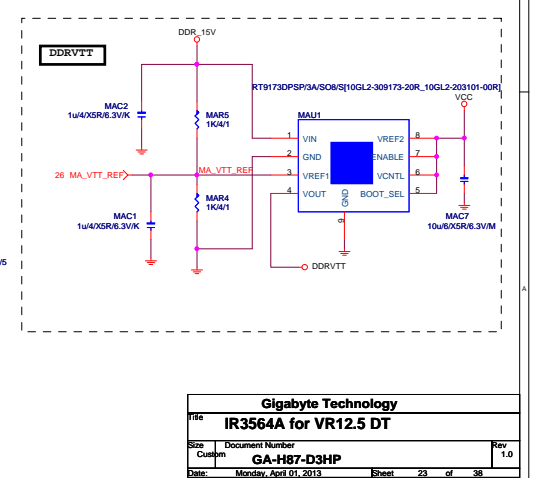
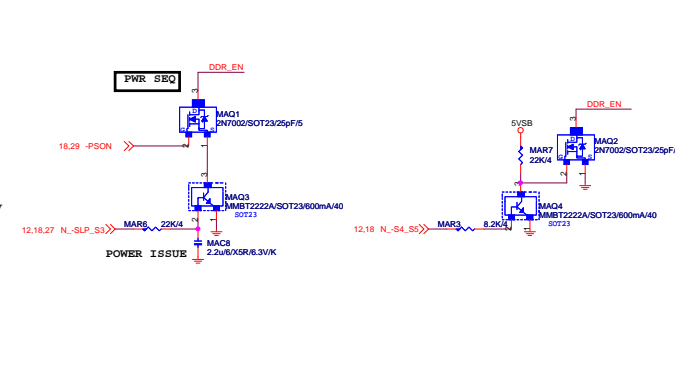
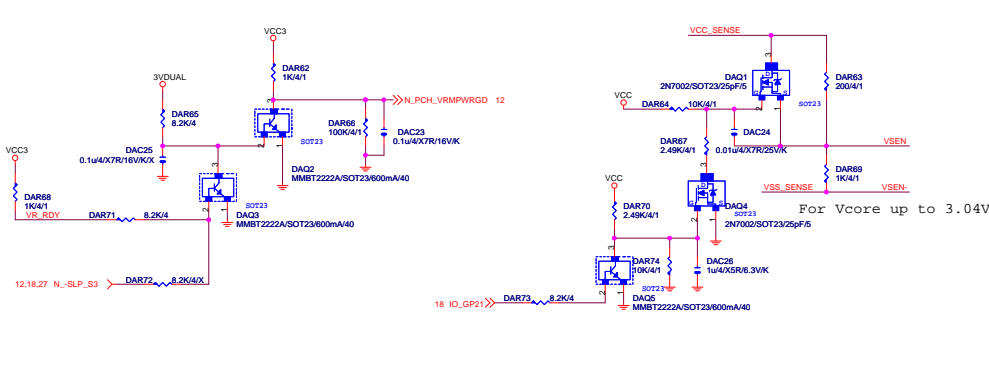
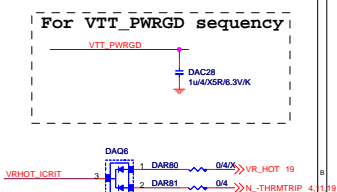
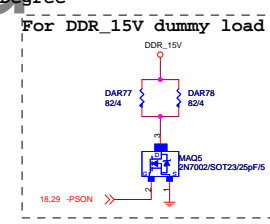
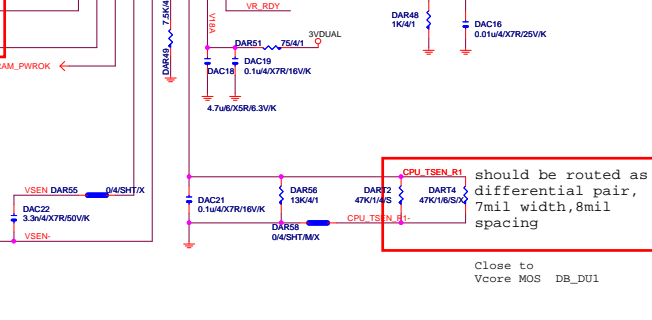
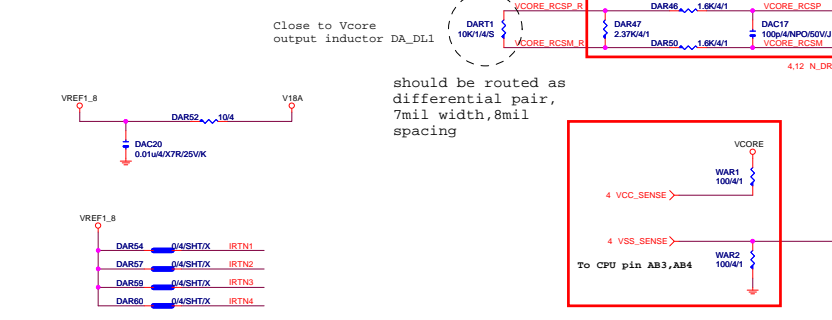
To CPU pin AB3,AB4

Debug Port



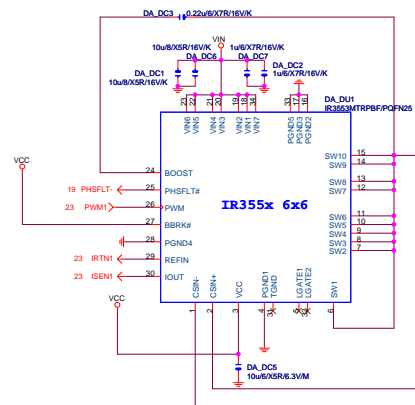
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OUP/UVP=250mV  
OCP=200A  
VRHOT=125 Degree  
OTP=130 Degree

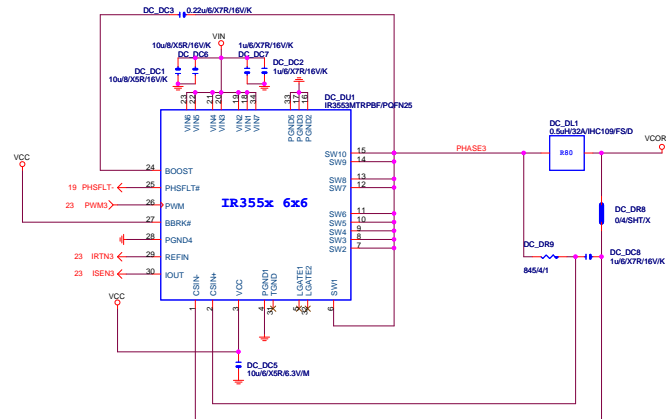


## VCORE

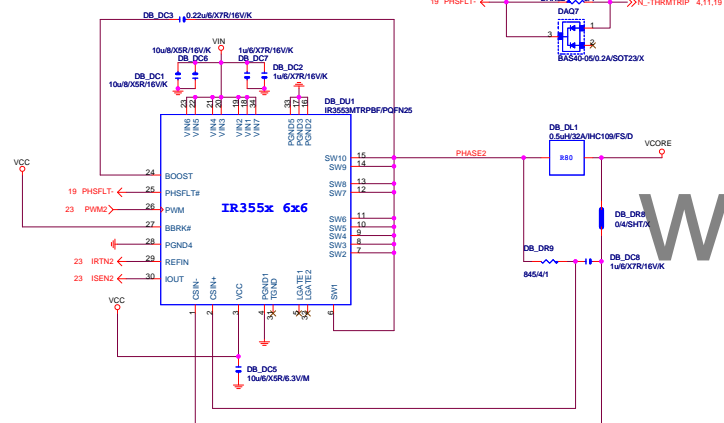
## VCORE-PHASE1



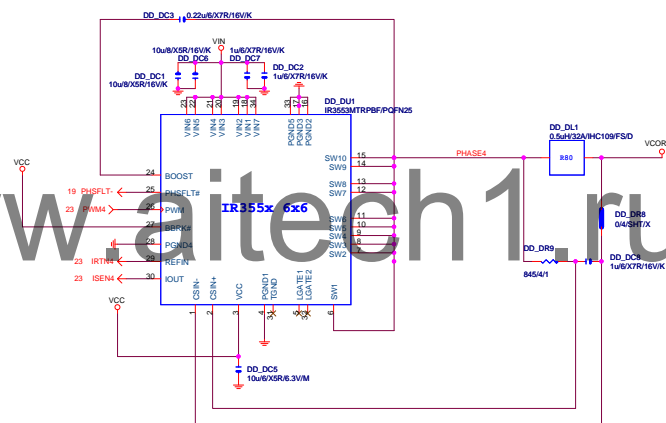
## VCORE-PHASE3



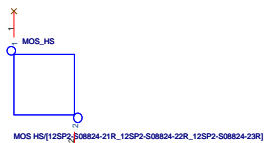
## VCORE-PHASE2



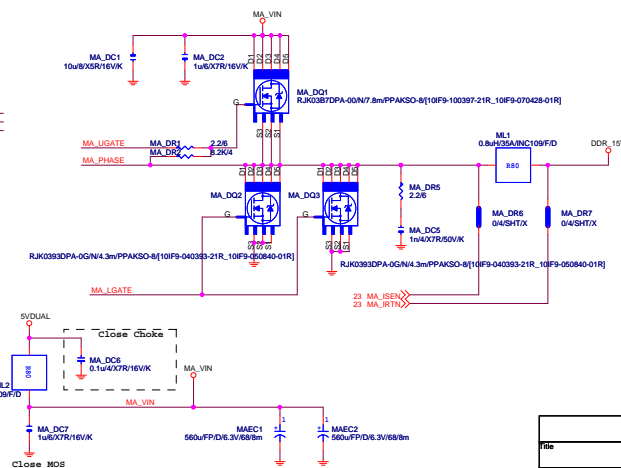
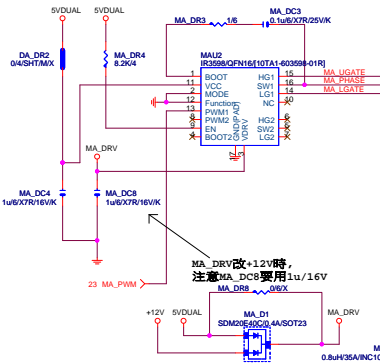
## VCORE-PHASE4



## MOSFET HEATSINK

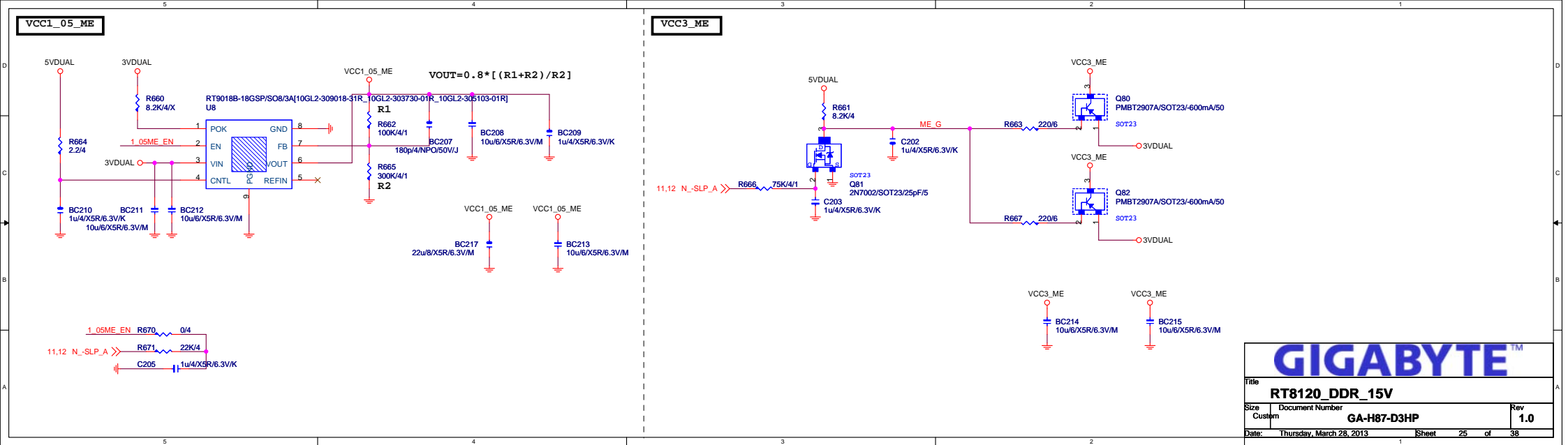


DDR\_15V



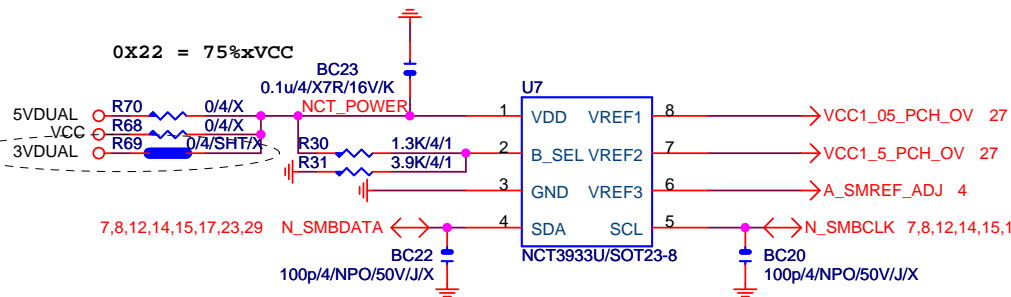
FUNCTION	MODE	PMN MODE	PHASE MODE
0	1	IR ATL	DUAL
1	1	IR ATL	Doubler
0	0	Tri-Seate	DUAL
1	0	Tri-Seate	Doubler
OPEN	0	Tri-Seate	Quad
CLOSE	1	TS ATL	Quad

In Quad mode , IC1 pin10 link to IC2 pin10  
IC1 pin9 link to IC2 pin9 without PU

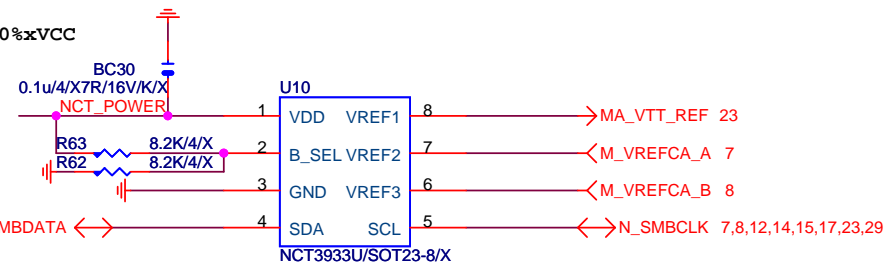


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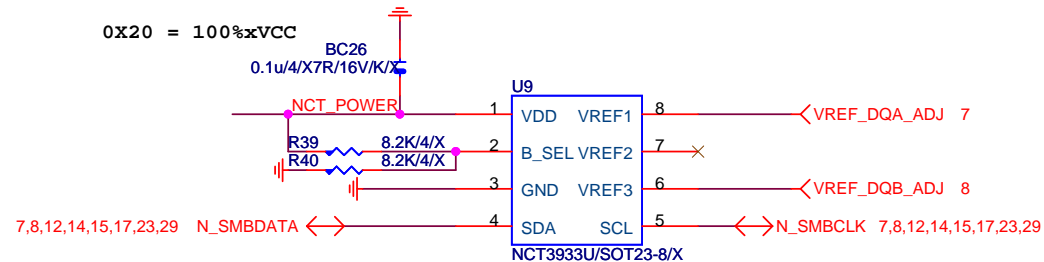
# OVER VOLTAGE



0X2A = 0%xVCC



0X20 = 100%xVCC

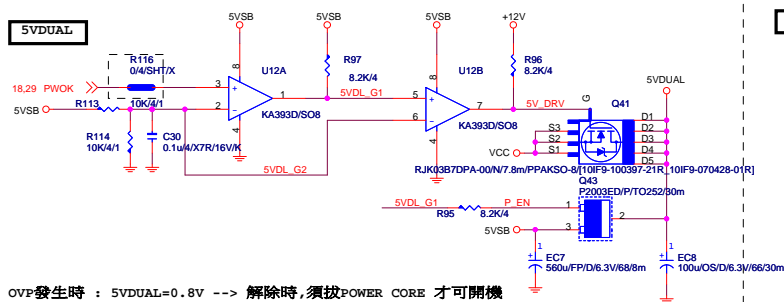


NCT3933	0X2A	0X20	0X22
VREF1	DDRVTT	VREF_DDRA_DQ	PCH Core
VREF2	VREF_DDRA_CA	N/A	VCC1_5_PCH
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	SMREF

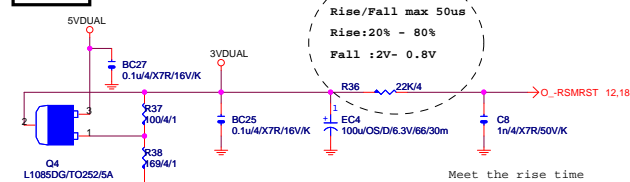
Gigabyte Technology

Title		
CPU CORE VR-2		
Size	Document Number	Rev
Custom	GA-H87-D3HP	1.0
Date:	Monday, April 01, 2013	Sheet 26 of 38

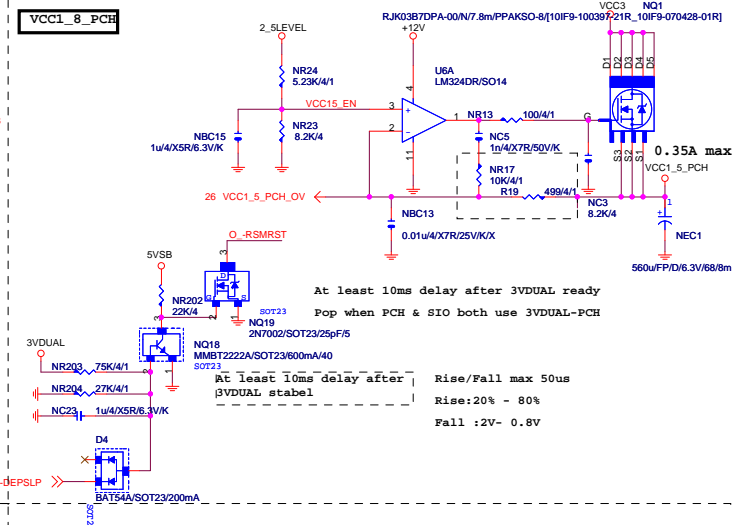
# 5VDUAL



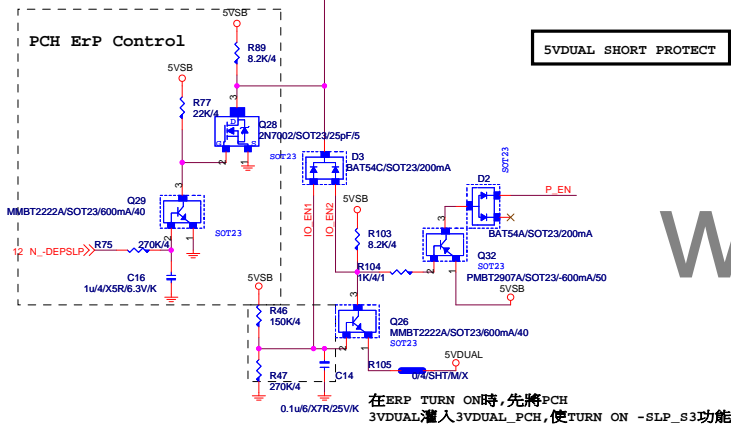
# 3VDUAL



# VCC1\_8\_PCH

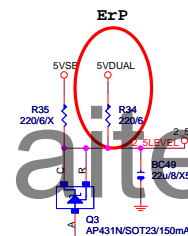


# PCH ErP Control

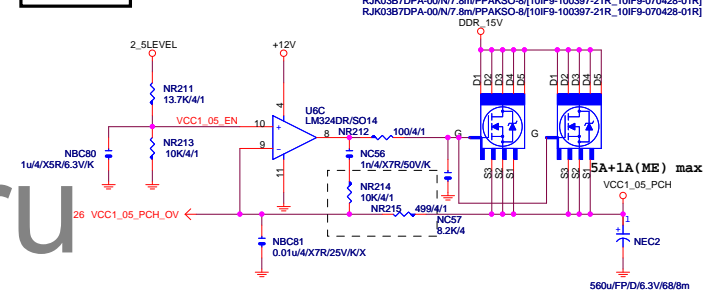


# 5VDUAL SHORT PROTECT

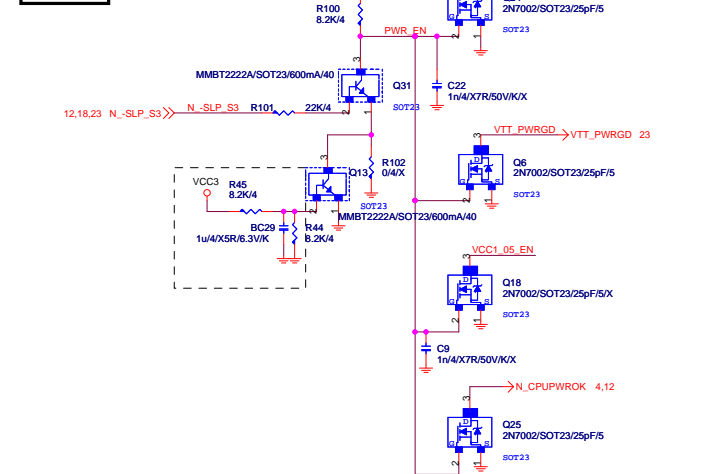
# 2\_5LEVEL



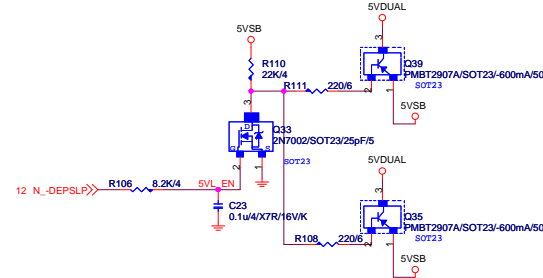
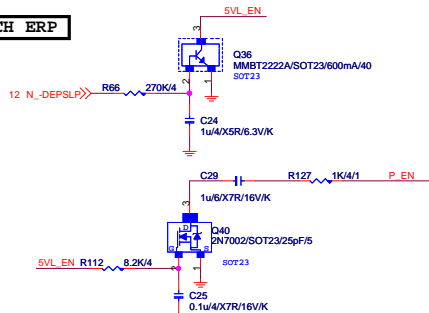
# VCC1\_05\_PCH



# PWR\_SEQ

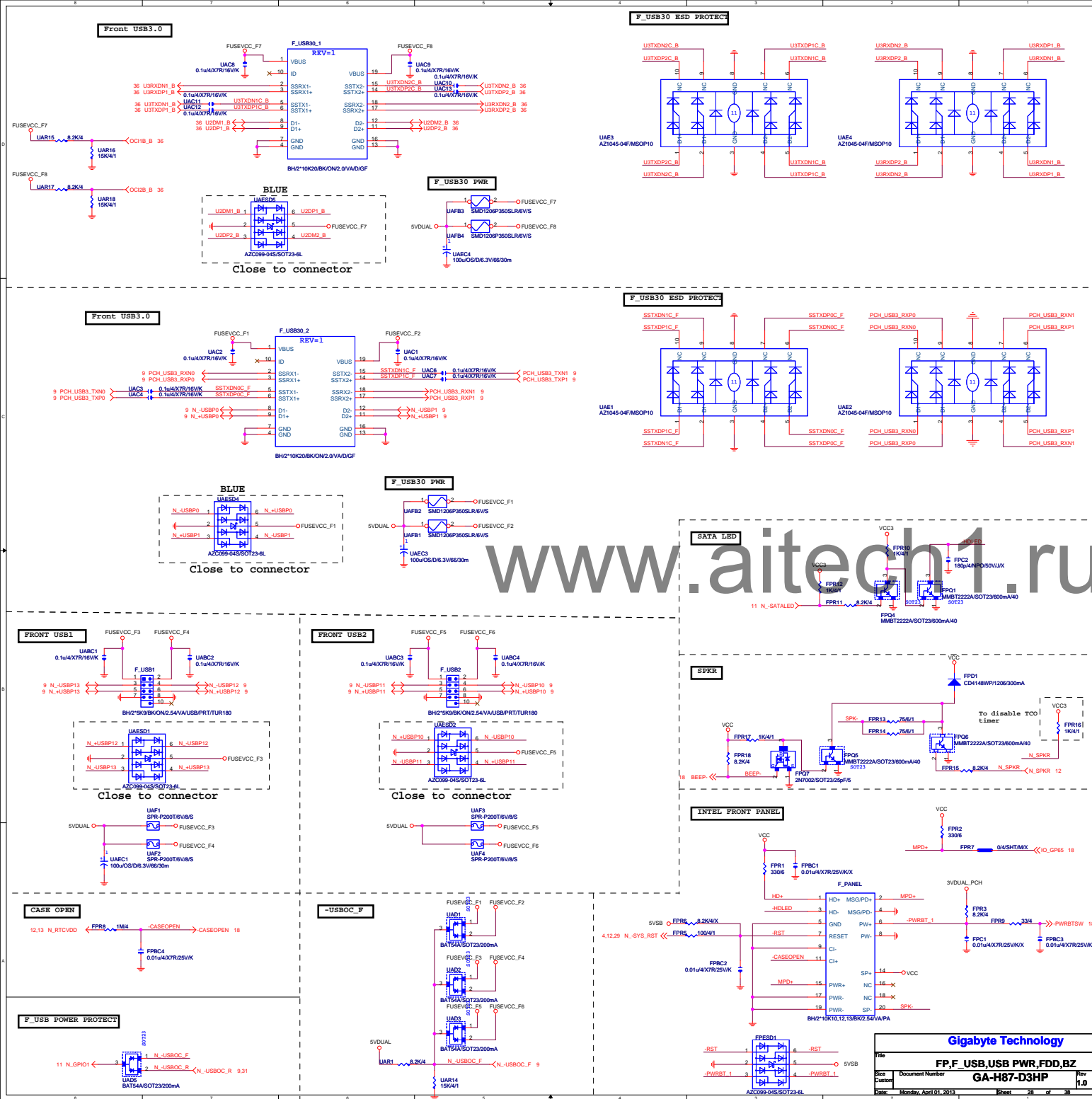


# PCH ERP

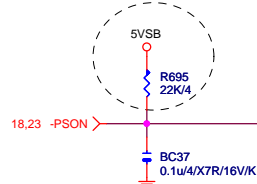


Gigabyte Technology

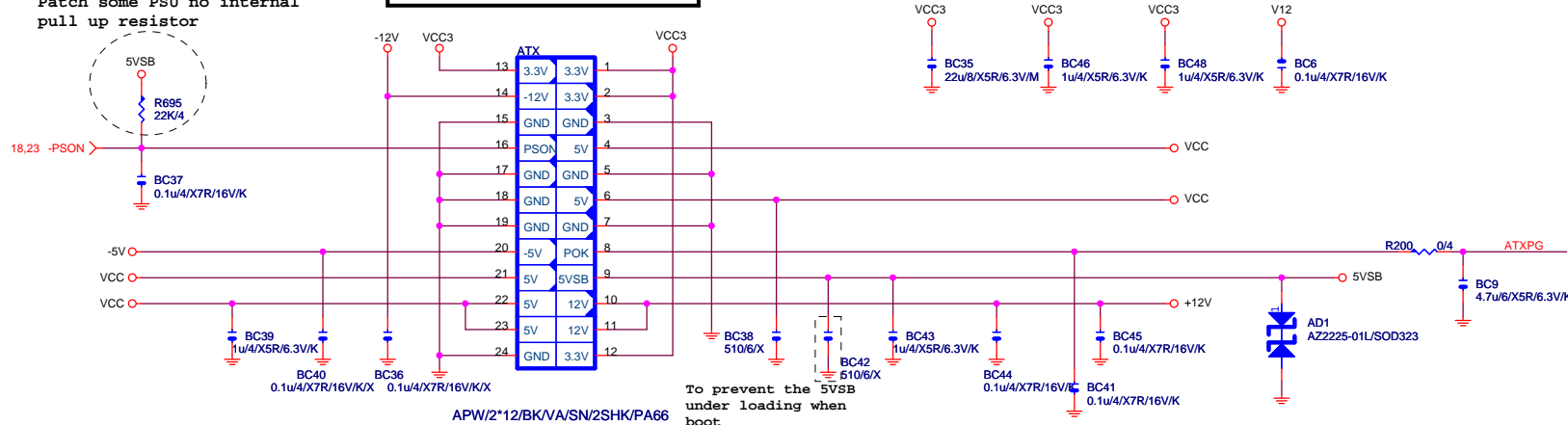
Title		
DISCRETE POWER		
Size	Document Number	Rev
Custom	GA-H87-D3HP	1.0
Date:	Monday, April 01, 2013	Sheet 27 of 38



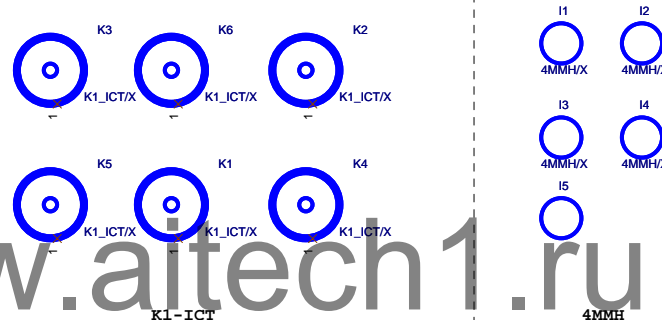
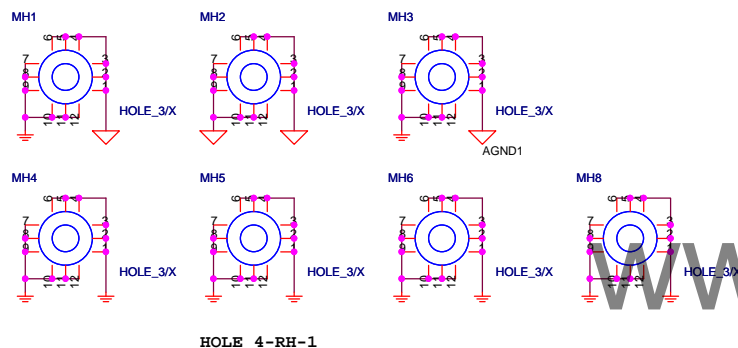
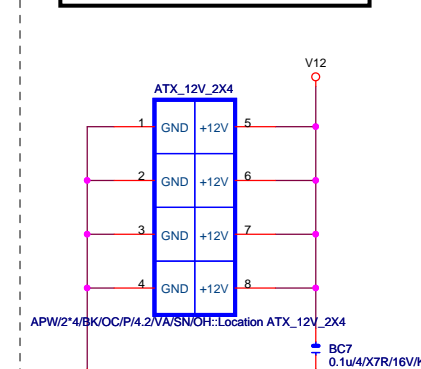
Patch some PSU no internal pull up resistor



## ATXX24 POWER CONNECTOR

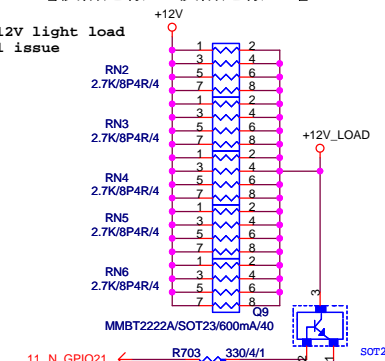


## ATXX4 POWER CONNECTOR



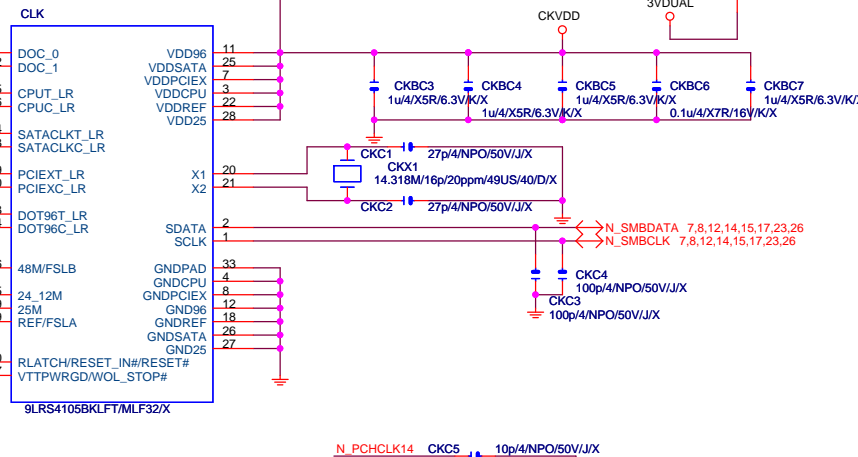
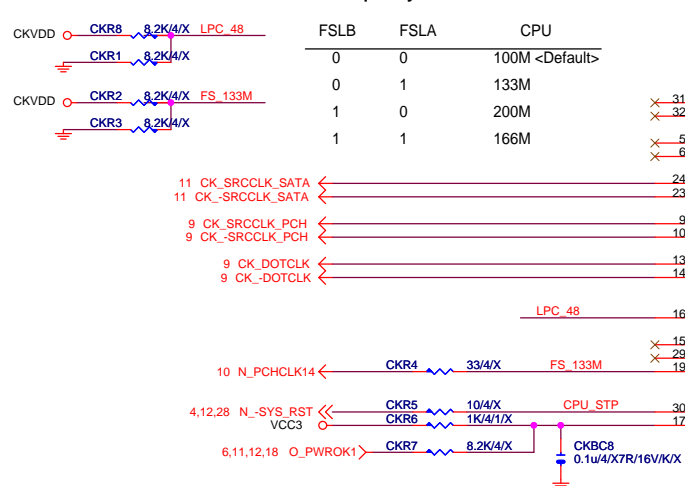
## 【技術通報R&D技術通報153】

To fix 12V light load abnormal issue



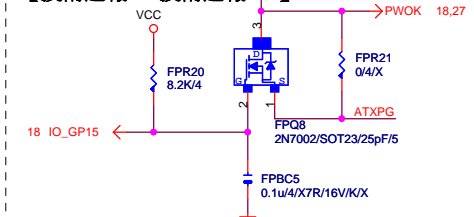
## CLK GEN

### CPU Frequency Selection



## PWOK PATCH

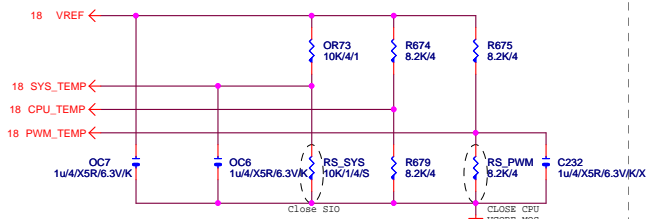
### 【技術通報R&D技術通報154】



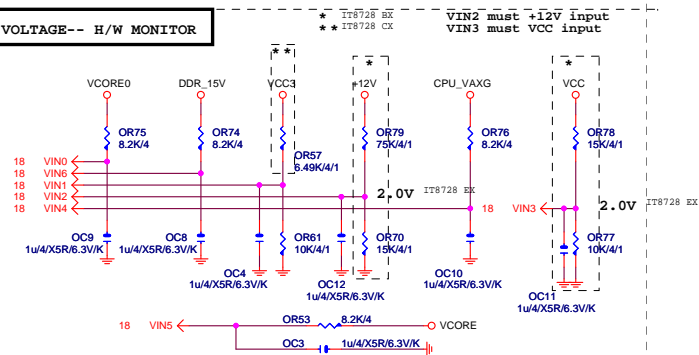
## Gigabyte Technology

Title			ATX POWER CONNECTOR
Size	Document Number	GA-H87-D3HP	
Custom		Rev 1.0	
Date	Monday, April 01, 2013	Sheet	29 of 38

## TEMP H/W MONITOR

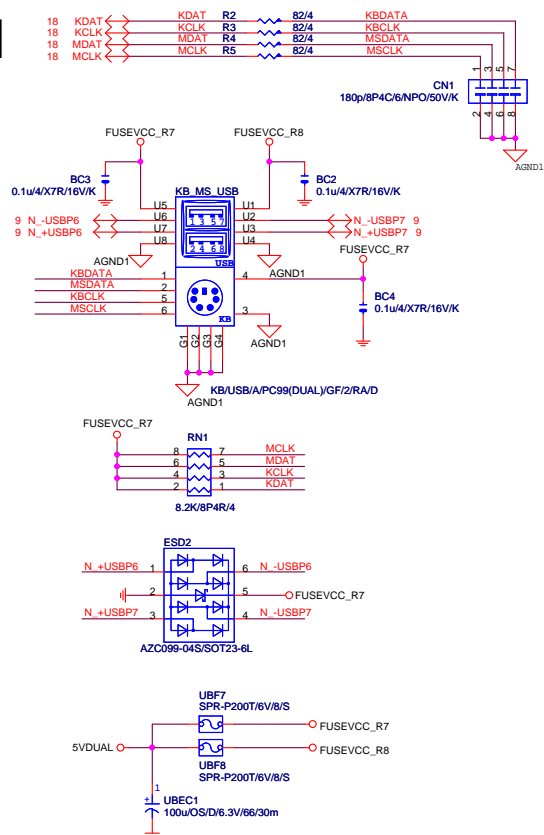


VOLTAGE-- H/W MONITOR

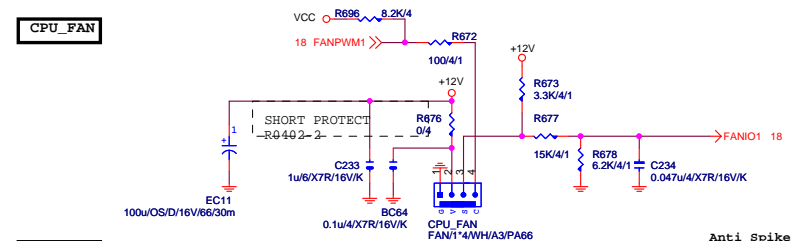


The division voltage of VIN2 & VIN3 must be around 2.9V

## KB/USB

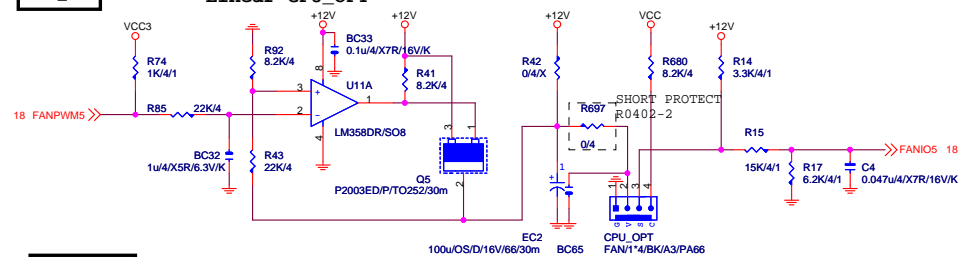


## CPU\_FAN



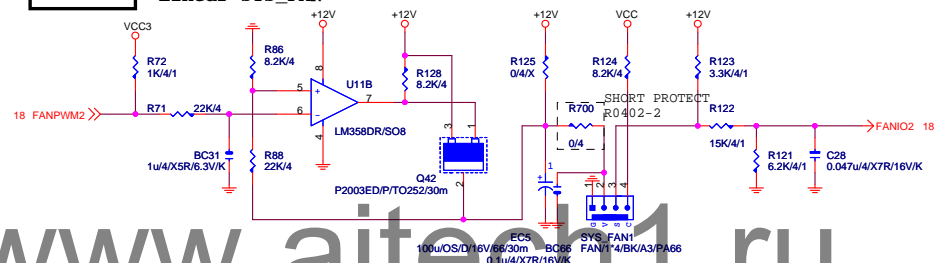
## CPU\_OPT

## Linear CPU OPT



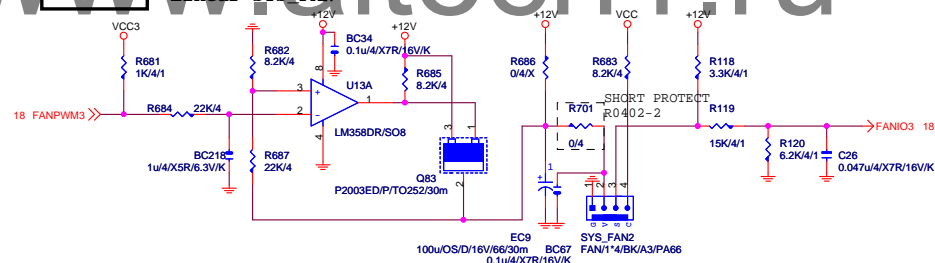
SYS_FAN_1	Linear SYS_FAN
-----------	----------------

Linear SYS\_FAN



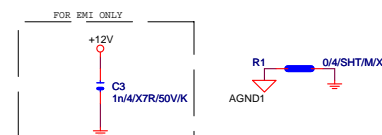
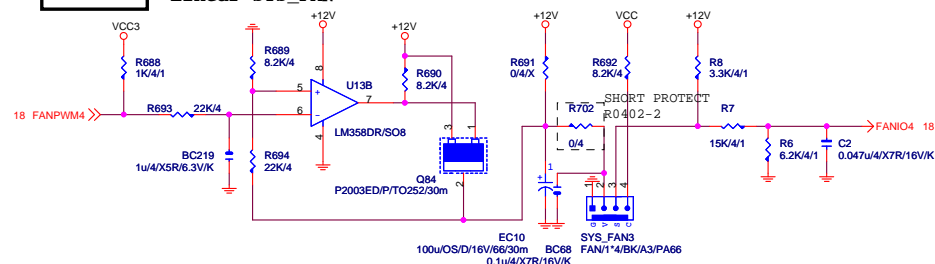
SYS\_FAN\_2 Linear SYS\_FAN

Linear SYS FA



## SYS FAN\_3 Linear SYS\_FA

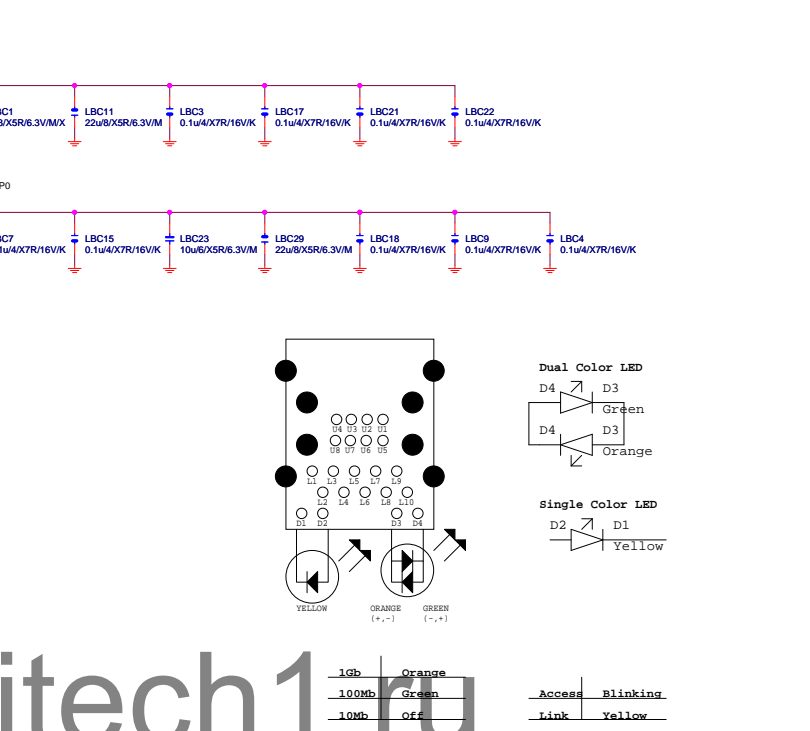
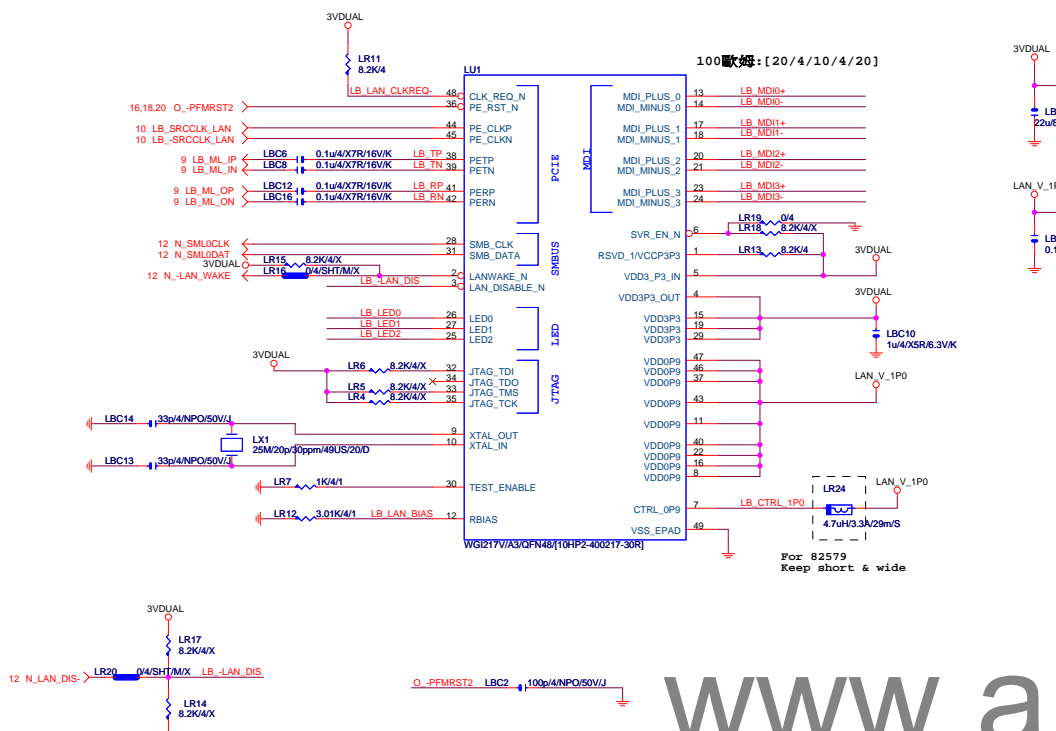
## Linear SYS\_FA



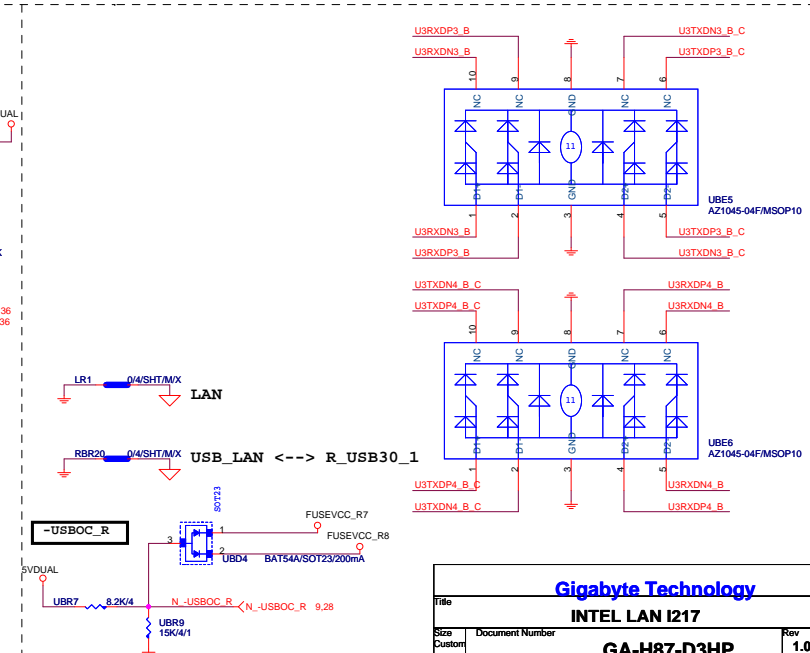
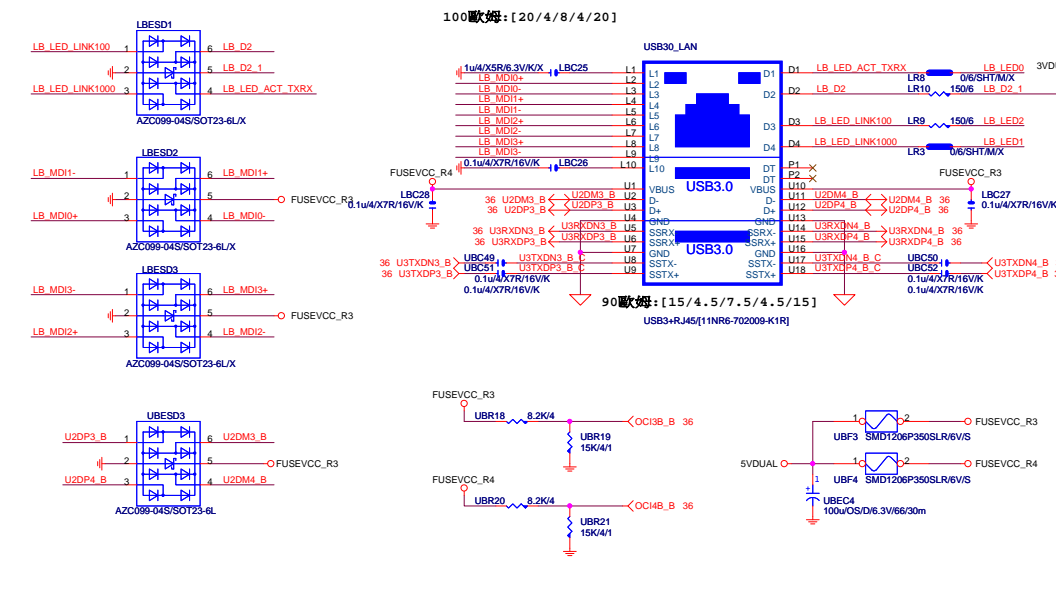
## Gigabyte Technology

Title				HWM,KB/MS, FAN CTRL			
Size	Document Number			Rev			
Custom	GA-H87-D3HP			1.0			
Date:	Monday, April 01, 2013			Sheet	30	of 38	

# LAN: INTEL I217

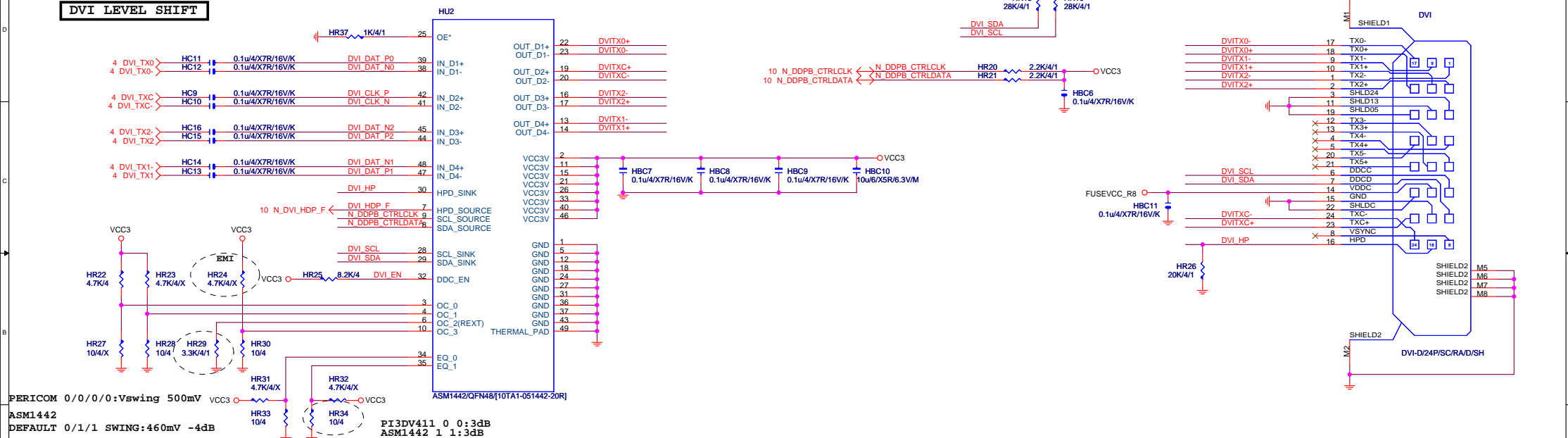


## USB30 LAN CONNECTOR



# DVI LEVEL SHIFT

DVI:15/4/4/15  
Impedance=85 +- 17.5%



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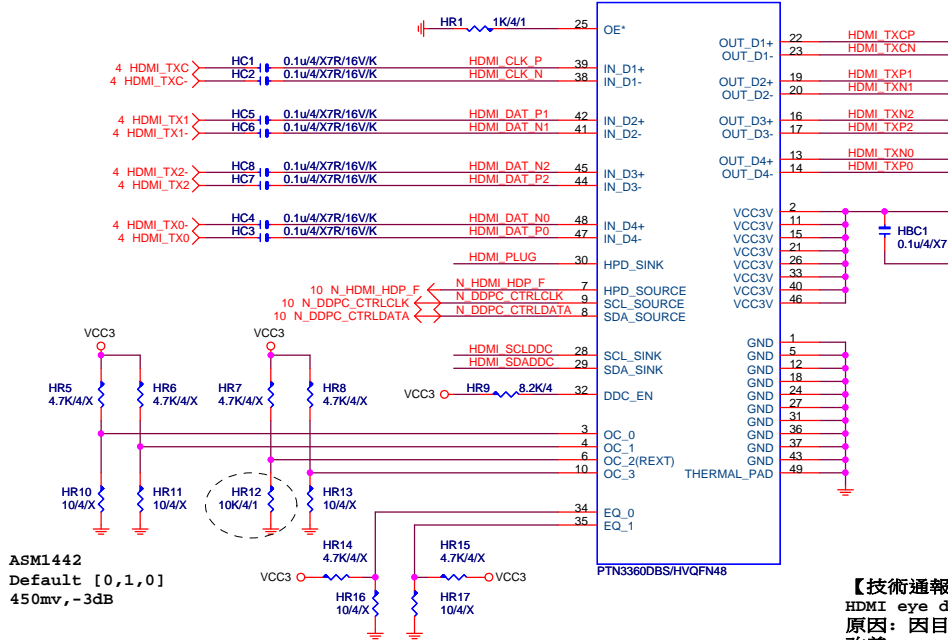
Gigabyte Technology			
TI TSB43AB23 1394			
Size Custom	Document Number	GA-H87-D3HP	
Date: Monday, April 01, 2013	Sheet	32	of 38
		Rev	1.0

# HDMI LEVEL SHIFT

HDMI:15/4/4/15

Impedance=85 +- 17.5%

HU1



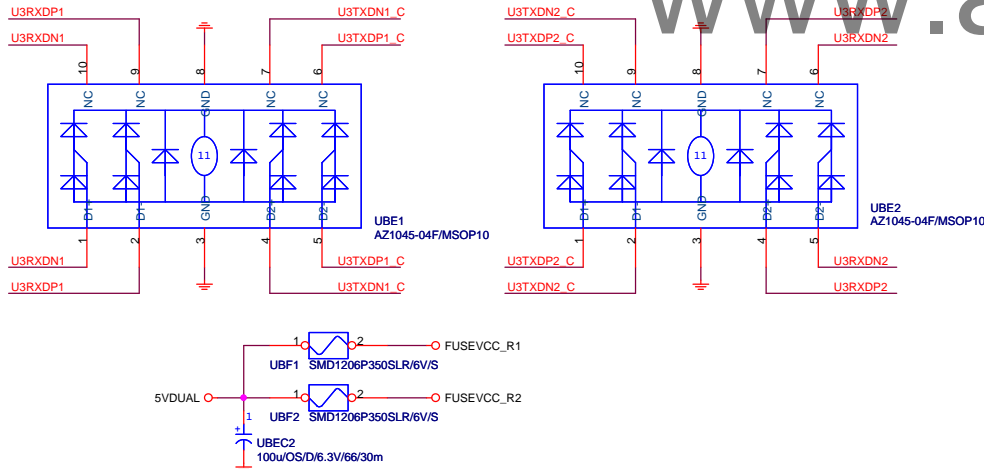
## 【技術通報R&D技術通報150】

HDMI eye diagram1.4版(deep color)會fail

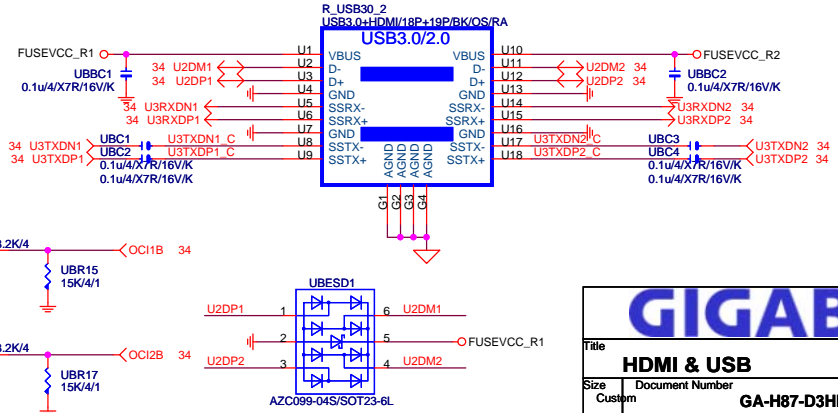
原因: 因目前的HDMI訊號過長,造成RISING TIME過慢,而會壓到eye diagram

改善: ASMEDIA ASML442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL DOWN電阻)

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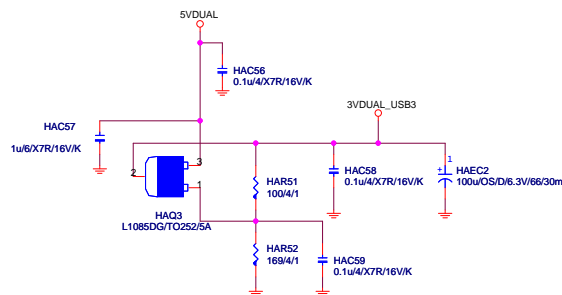
## R\_USB30



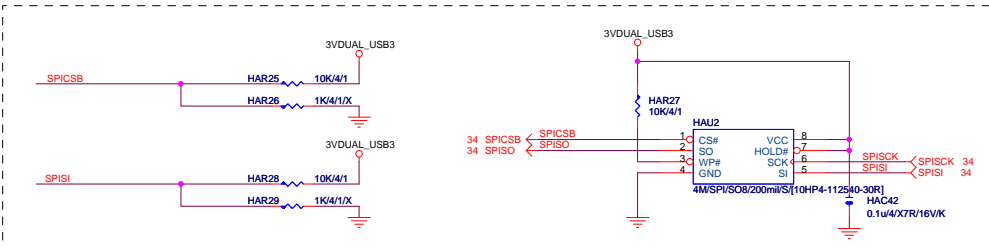
GIGABYTE™			
HDMI & USB			
File	Document Number	Rev	
	GA-H87-D3HP	1.0	
Date	Monday, April 01, 2013	Sheet	33 of 38



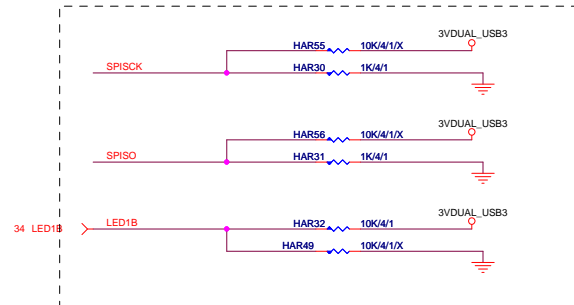
# 3VDUAL\_USB\_1



## # External SPI ROM ; SPI ROM attached mode

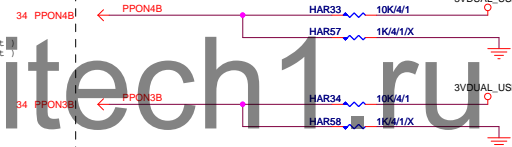


## # Battery Charging

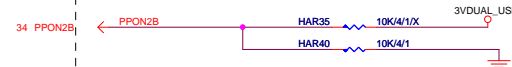


## # Number of Ports ; 4Ports mode

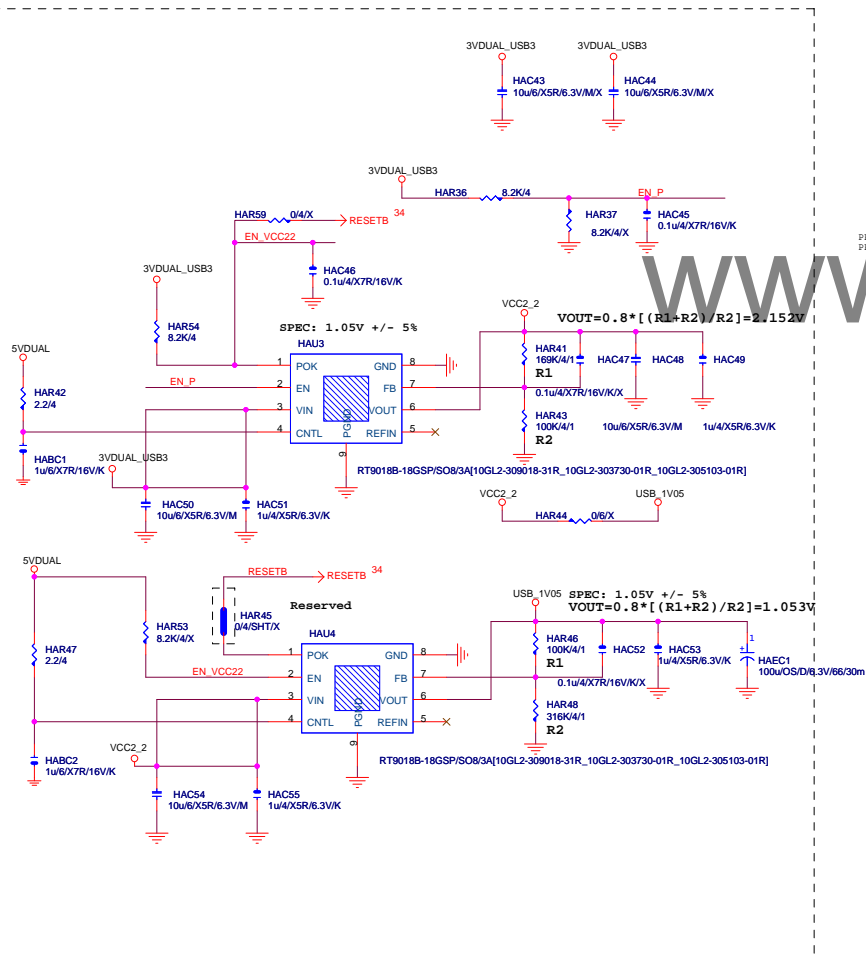
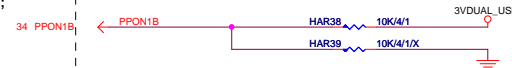
PPON3B / PPO4B : H / H ( 4 port )  
PPON3B / PPO4B : L / L ( 2 port )

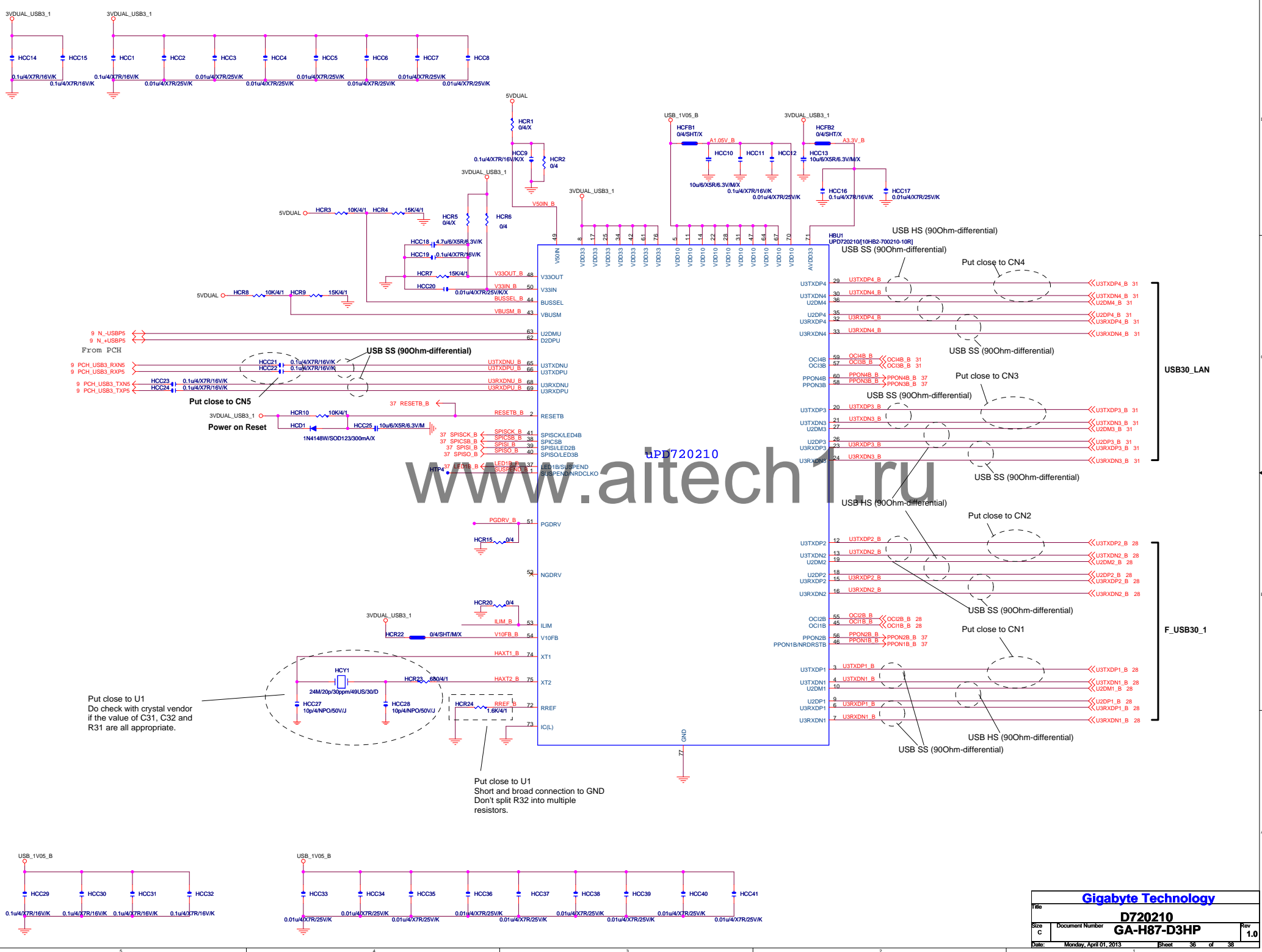


## #5 VBUS Power Control ; Individual mode

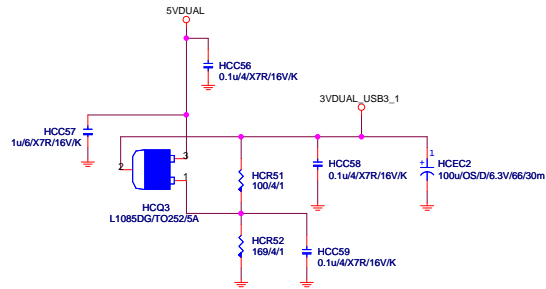


## # PPON1B Pin Function ; Port1 PPONB mode

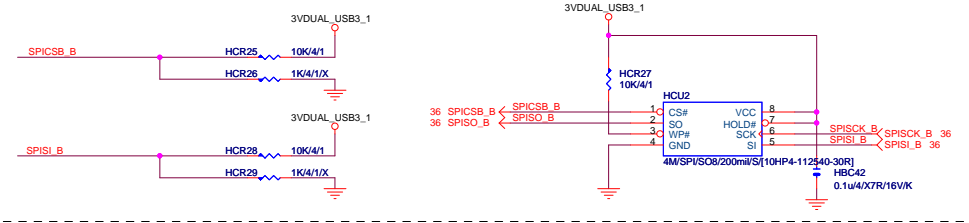




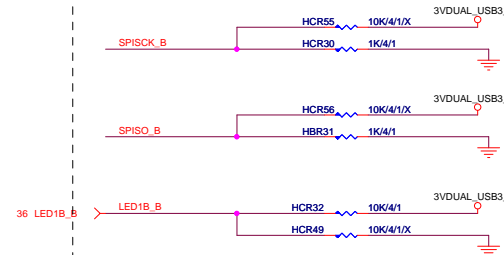
### 3VDUAL\_USB\_2



### # External SPI ROM ; SPI ROM attached mode

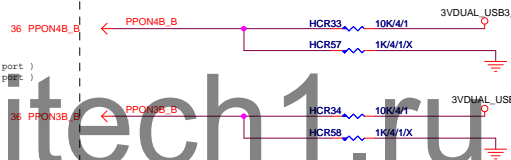


### # Battery Charging

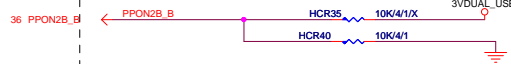


### # Number of Ports ; 4Ports mode

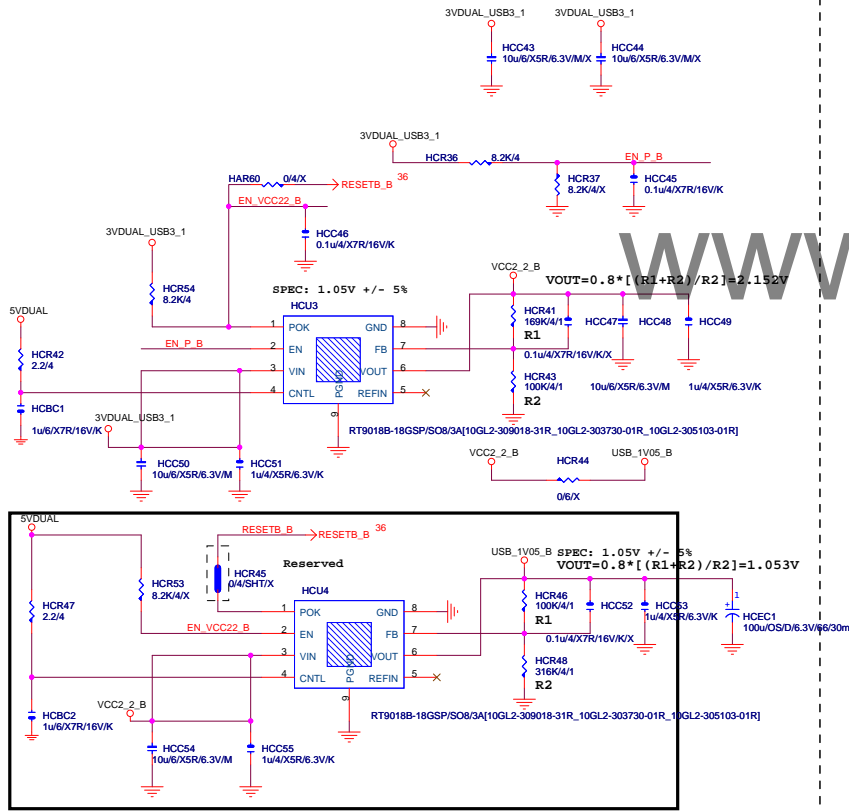
PPON3B / PPON4B : H / H ( 4 port )  
PPON3B / PPON4B : L / L ( 2 port )



### #5 VBUS Power Control ; Individual mode



### # PPON1B Pin Function ; Port1 PPONB mode



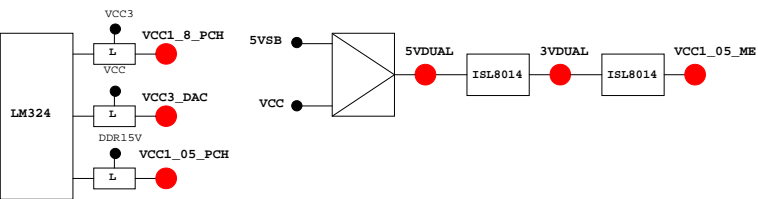
PCB GPIO LIST TABLE

PIN NAME	PWR	Default	USAG	NOTE
GP0	MAIN	H-Z	GPIO0	N/A
GP1/TACH1	MAIN	GPI	GPIO1	N/A
GP2/PIRQE#	MAIN	GPI	~PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN	GPI	~PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN	GPI	~PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN	GPI	~PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN	GPI	PCIEX1 Detect	P/U 8.2K VCC3
GP7/TACH3	MAIN	GPI	GPIO7	P/U 8.2K VCC3
GP8	STBY	H	GPI	GPIO8
GP9/OC5#	STBY	NATIVE	USB OC5#	N/A
GP10/OC6#	STBY	NATIVE	USB OC6#	N/A
GP11/SMBALERT#	STBY	NATIVE	USB PWR protect	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	GPIO12
GP13	STBY	L	GPI	LPCPME#
GP14/OC7#	STBY	NATIVE	USB OC7#	N/A
GP15	STBY	L	GPI	GPIO15(TLS Enable)
GP16	MAIN	GPI	GPIO16	P/U 8.2K VCC3
GP17/TACH0	MAIN	GPI	GPIO17	P/U 8.2K VCC3
GP18	MAIN	GPI	Mobile Only	N/A
GP19	MAIN	GPI	GPIO19	P/U 8.2K VCC3
GP20	MAIN	GPI	GPIO20	P/U 8.2K VCC3
GP21	MAIN	GPI	GPIO21	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	GPIO22
GP23	MAIN	GPI	GPIO23	N/A
GP24	STBY	L	GPI	SKTOCC#
GP25	STBY		Mobile Only	N/A
GP26	STBY		Mobile Only	N/A
GP27	STBY	H	GPO	GPIO27
GP28	STBY	H	GPO	PWR LED
GP29	STBY	L	GPI	GPIO29
GP30	STBY	H-Z	GPI	Mobile Only
GP31	STBY	H-Z	GPI	Mobile Only
GP32	MAIN	H	GPO	N/A
GP33	MAIN	H	GPO	N/A
GP34	MAIN	H-Z	GPI	~PCI_STOP
GP35	MAIN	L	GPO	~ACZ_DET
GP36	MAIN	GPI	N/A	N/A
GP37	MAIN	GPI	N/A	N/A
GP38	MAIN	H-Z	GPI	PCIEX4 Detect
GP39	MAIN	H-Z	GPI	GPIO39
GP40	STBY	NATIVE	USB OC1#	N/A
GP41	STBY	NATIVE	USB OC2#	N/A
GP42	STBY	NATIVE	USB OC3#	N/A
GP43	STBY	NATIVE	USB OC4#	N/A
GP44	STBY	L	NATIVE	GPIO44
GP45	STBY	NATIVE	GPIO45	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	GPIO46
GP47	STBY		Mobile Only	N/A
GP48	MAIN	H-Z	IN	GPIO48
GP49	MAIN	H-Z	IN	GPIO49
GP50	MAIN	NATIVE	~REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	~GNT1
GP52	MAIN	NATIVE	~REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	~GNT2
GP54	MAIN	NATIVE	~REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	~GNT3
GP56	STBY	NATIVE	Mobile Only	N/A
GP57	STBY	H-Z	IN	VCORE_OV1
GP58	STBY	H-Z	NATIVE	F_USB_OC
GP59	STBY	NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)
GP61	STBY	L	NATIVE	~SUSTAT
GP62	STBY	L	NATIVE	SUSCLK
GP63	STBY	L	NATIVE	GPIO63
GP64	MAIN	L	NATIVE	CLKOUTFLEX0
GP65	MAIN	L	NATIVE	CLKOUTFLEX1
GP66	MAIN	L	NATIVE	CLKOUTFLEX2
GP67	MAIN	L	NATIVE	CLKOUTFLEX3
GP72	STBY	H-Z	NATIVE	VCORE_OV4
GP73	STBY		Mobile Only	N/A
GP74	STBY	H-Z	NATIVE	1_05V_OV2
GP75	STBY	H-Z	NATIVE	N/A(Reverse)

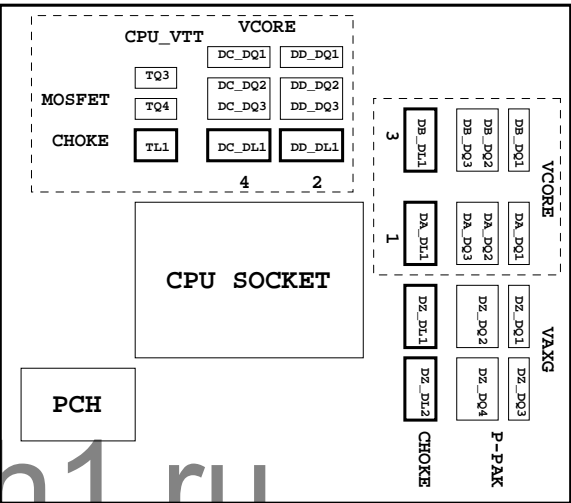
Super I/O ITE8720 GPIO Table

PIN NAME	USAG	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRX1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAG	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/SEN	LOW_PWR_1	
VIDO5/GP27/SEN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSB5W#/GP40	CSI_F0	BSEL166_1
SUSCH#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AFD#/GP86/SMB_C_R	SEN_PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	NBT_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMB_C_M	DDR_LED3_C	
PWRON#/GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRX2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下:



BIOS超電壓對應表:

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Termination
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

散熱模組料號:

Z77-D3H :  
PCH :  
12SP2-S05511-01R/02R/03R  
MOSFET :  
12SP2-S08924-01R/02R/03R

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

Gigabyte Technology			
TABLE LIST			
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